



WELCOME To

ISSCC 2014 SESSION 11

DATA CONVERTER TECHNIQUES

An Oversampled 12/14b SAR ADC with Noise Reduction and Linearity Enhancements Achieving up to 79.1dB SNDR

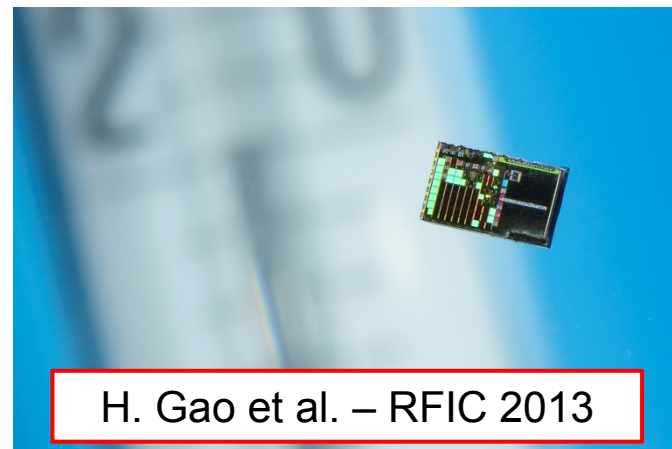
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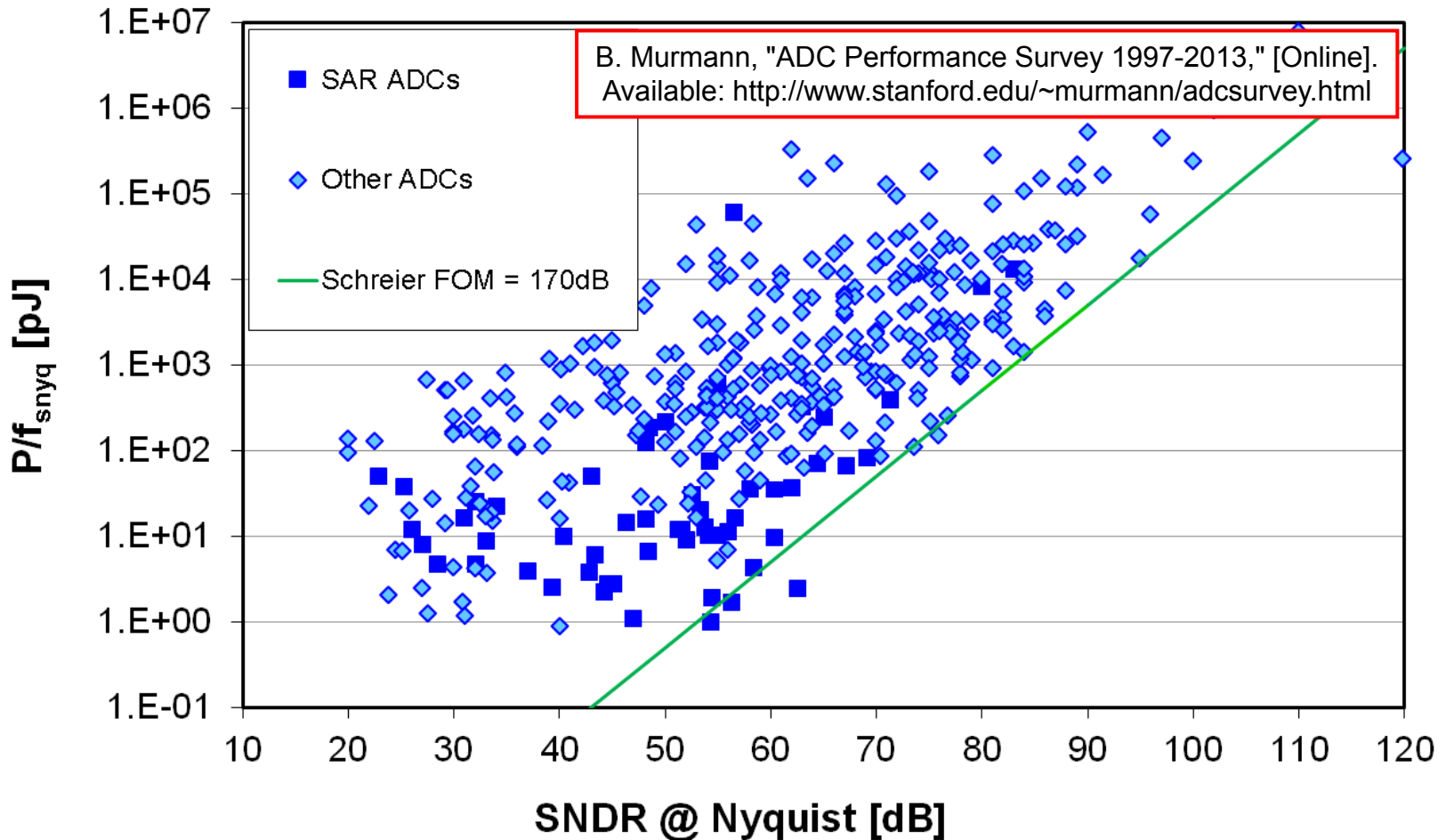
Application

- Wireless sensor networks
 - Environmental monitoring
 - Bio-potential recording

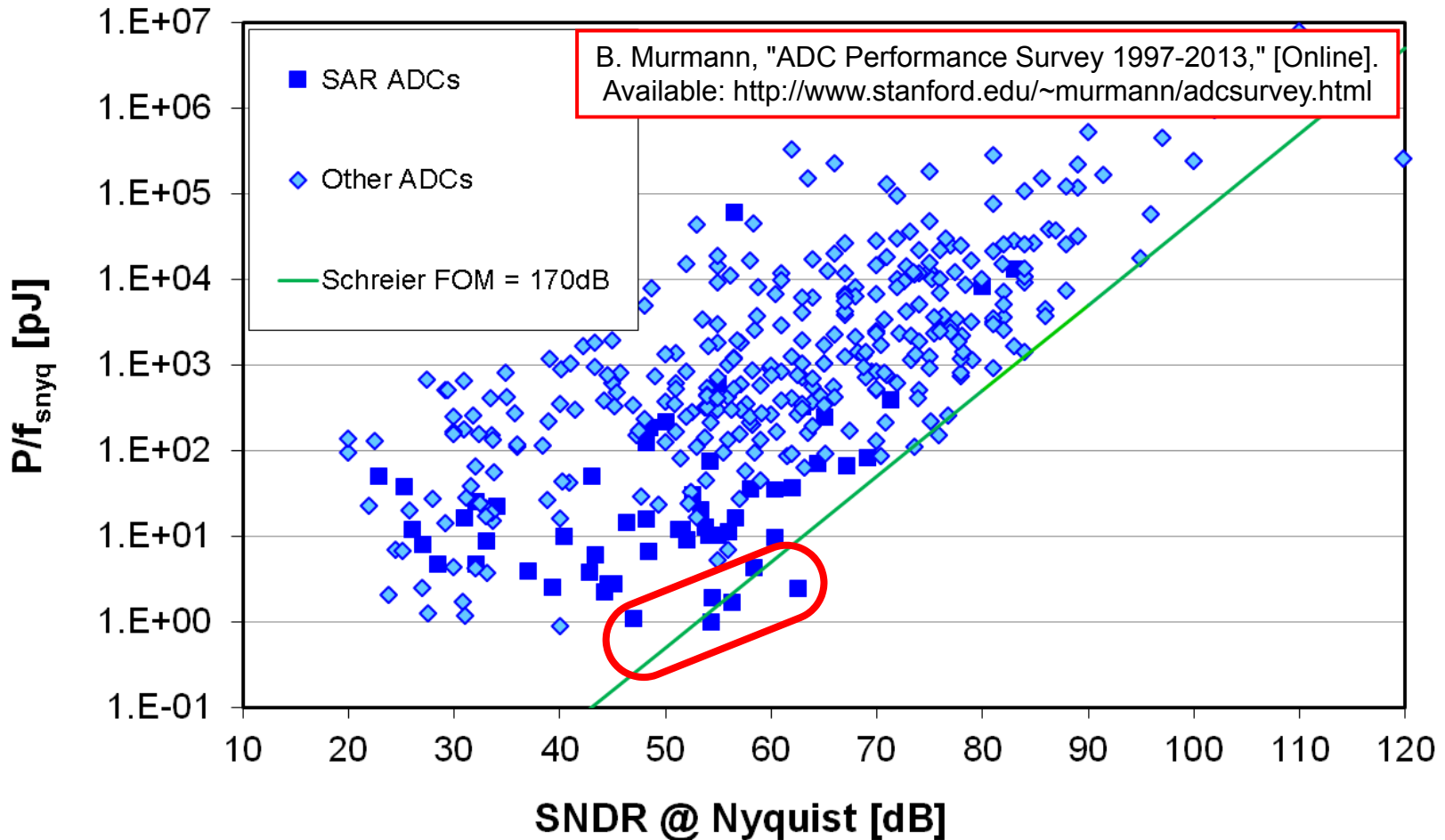


- Typical ADC specifications
 - Relatively low speed $\sim 1 - 10\text{kHz BW}$
 - Relatively high resolution $\sim 10 - 14 \text{ bit}$
 - Very low power $\sim 1\mu\text{W}$

Prior-Art Low-Power ADCs

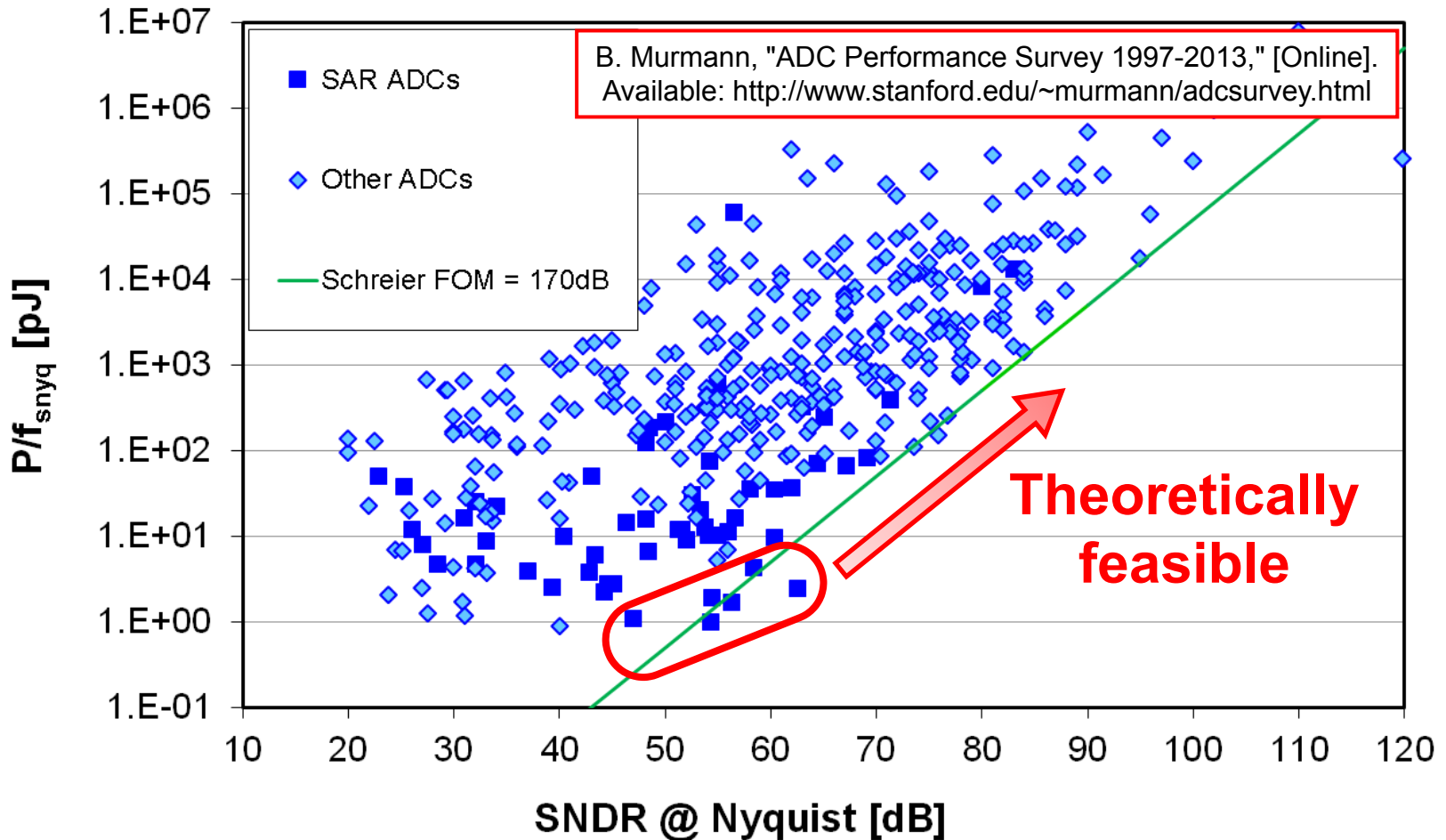


Prior-Art Low-Power ADCs

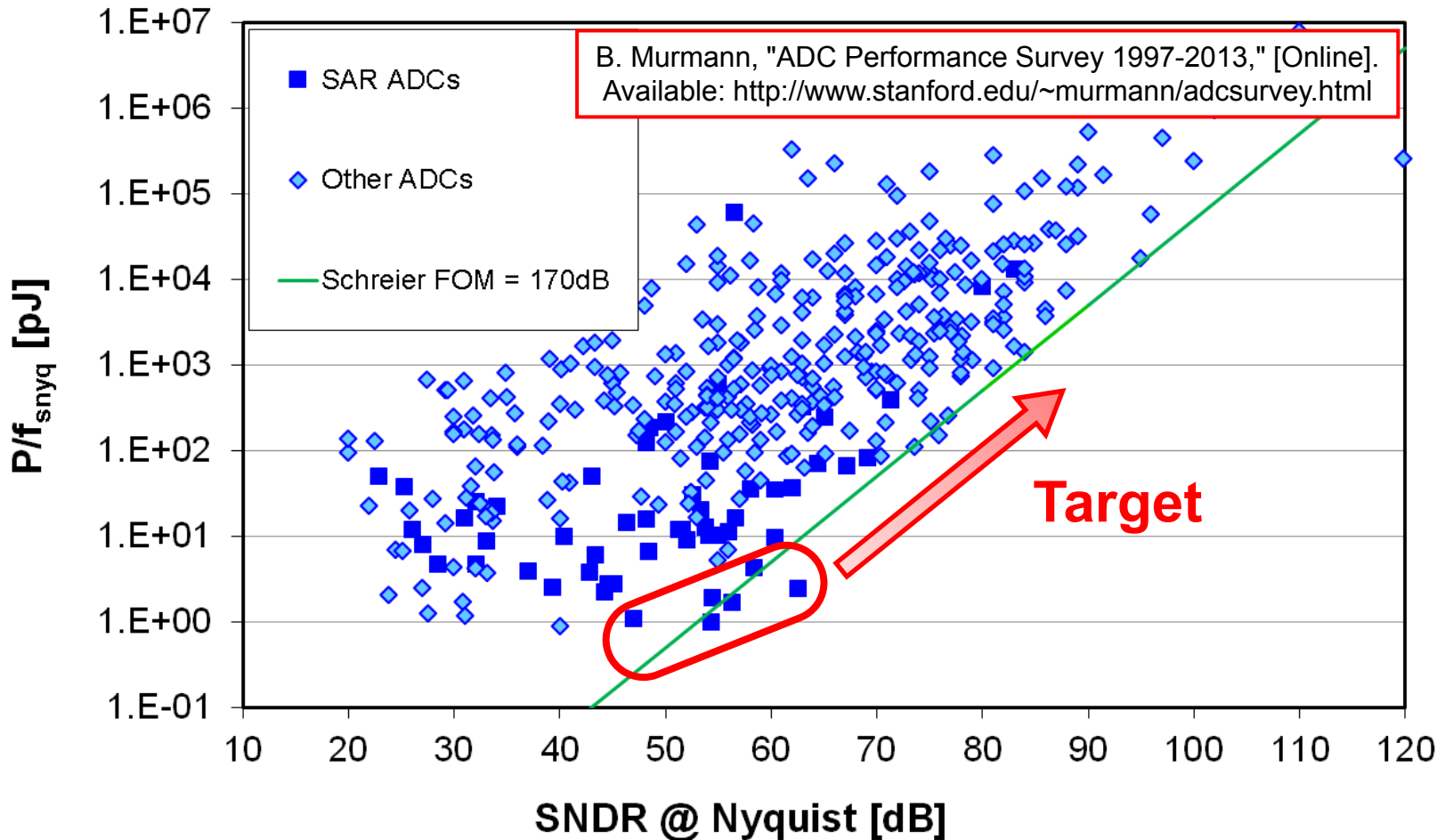


- Low-power SAR: limited to 45 ~ 62dB SNDR

Prior-Art Low-Power ADCs



Prior-Art Low-Power ADCs



- Target is feasible theoretically but difficult in reality

Challenges and Solutions

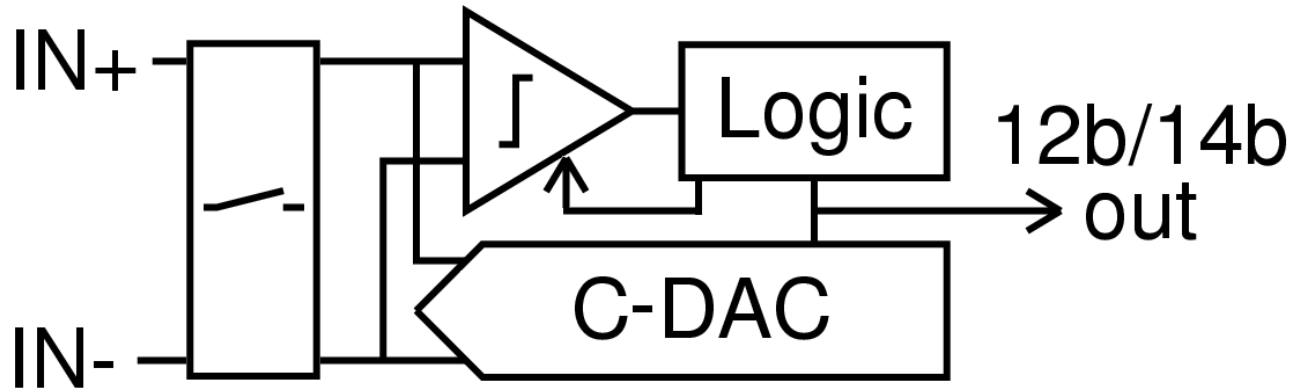
	White Noise	1/f Noise	INL/DNL-Induced Distortion
Data-Driven Noise Reduction			
Oversampling			
Chopping			
Dithering			

- Final result:
SNDR 79.1dB, SFDR 87.1dB, SNR 86.8dB

Outline

- SAR ADC core
 - DAC implementation
- Oversampling
 - Chopping
 - Dithering
- Feedback-Controlled Data-Driven Noise Reduction
- Measurement results
- Conclusions

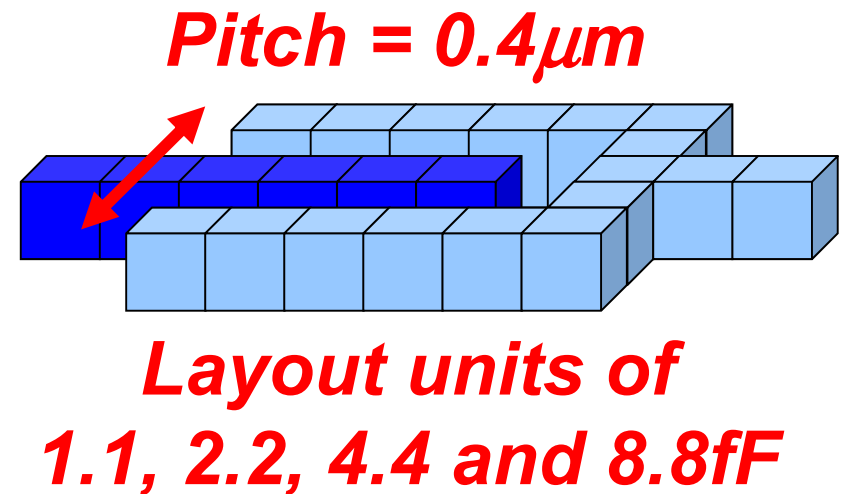
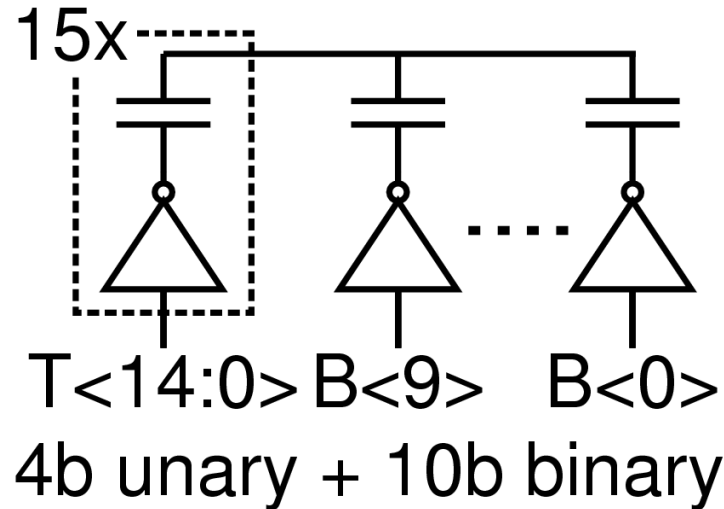
SAR ADC Core Architecture



- Supports 12 & 14-bit resolution
- Single 0.8V supply / reference
- Self-synchronized (requires clock @ f_{sample} only)
- Max. sample rate of 128kS/s

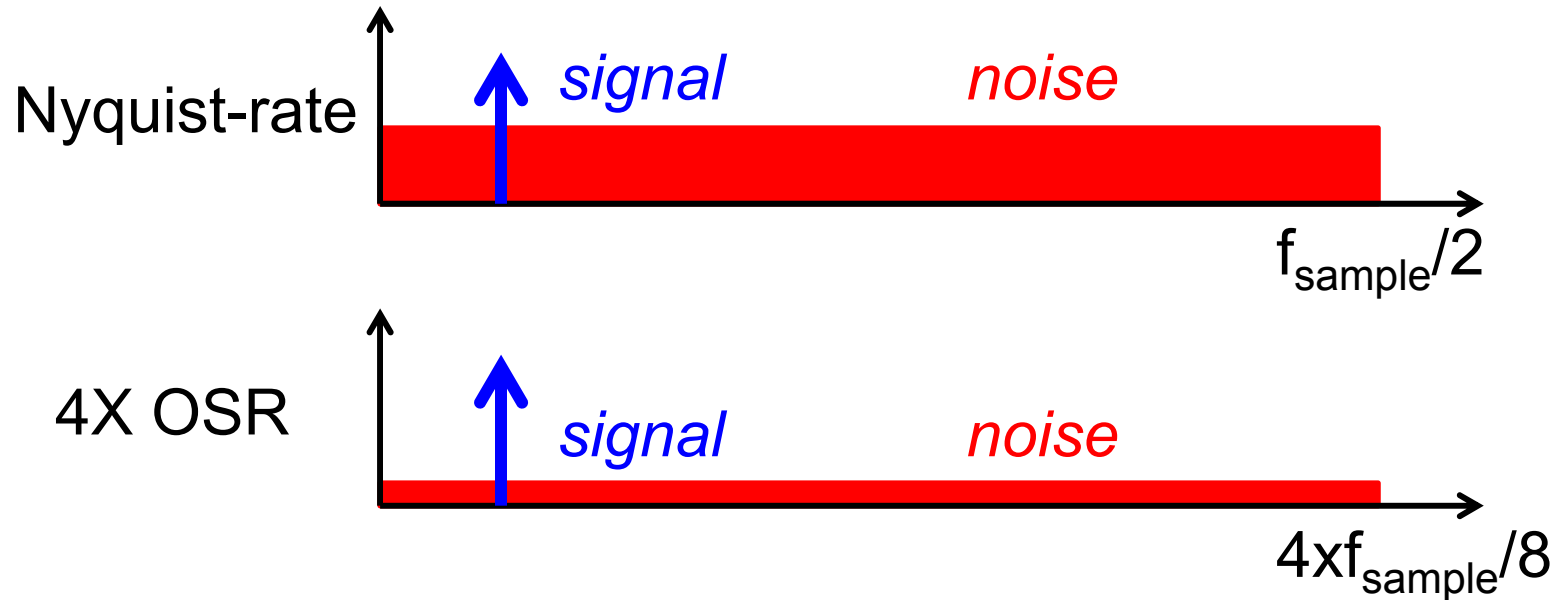
14b Charge Redistribution DAC

- 9pF per side for 85dB kT/C-SNR
- 14b resolution: 4b unary MSBs + 10b binary LSBs



Bit	T<14..0>	B<9..4>	B<3>	B<2>	B<1>	B<0>
Unit	8.8fF	8.8fF	4.4fF	2.2fF	1.1fF	1.1fF
#Units	64 (15X)	32, 16, 8, 4, 2, 1	1	1	1	1/2

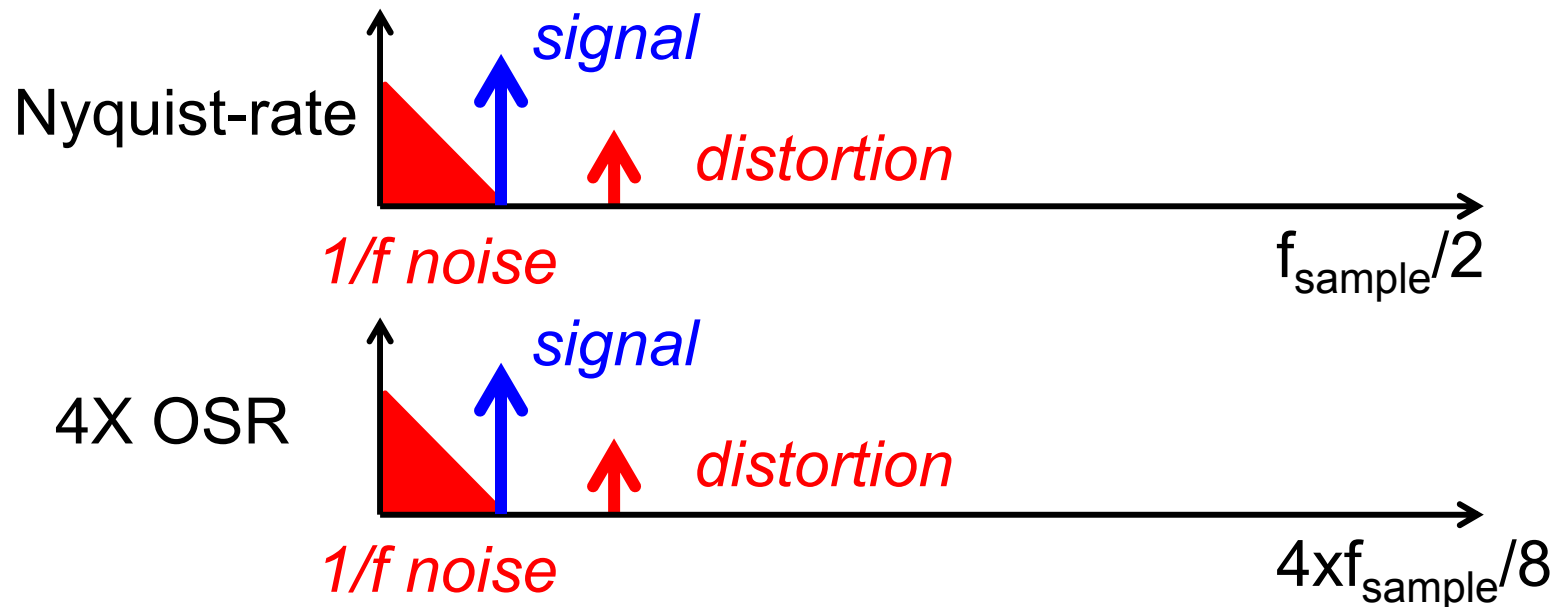
Oversampling



- 4X oversampling (i.e. 4X power) \rightarrow +6dB SNR \rightarrow Constant Schreier-FOM scaling
- Helps for thermal noise and quantization noise (if sufficiently uncorrelated to the signal)

Oversampling

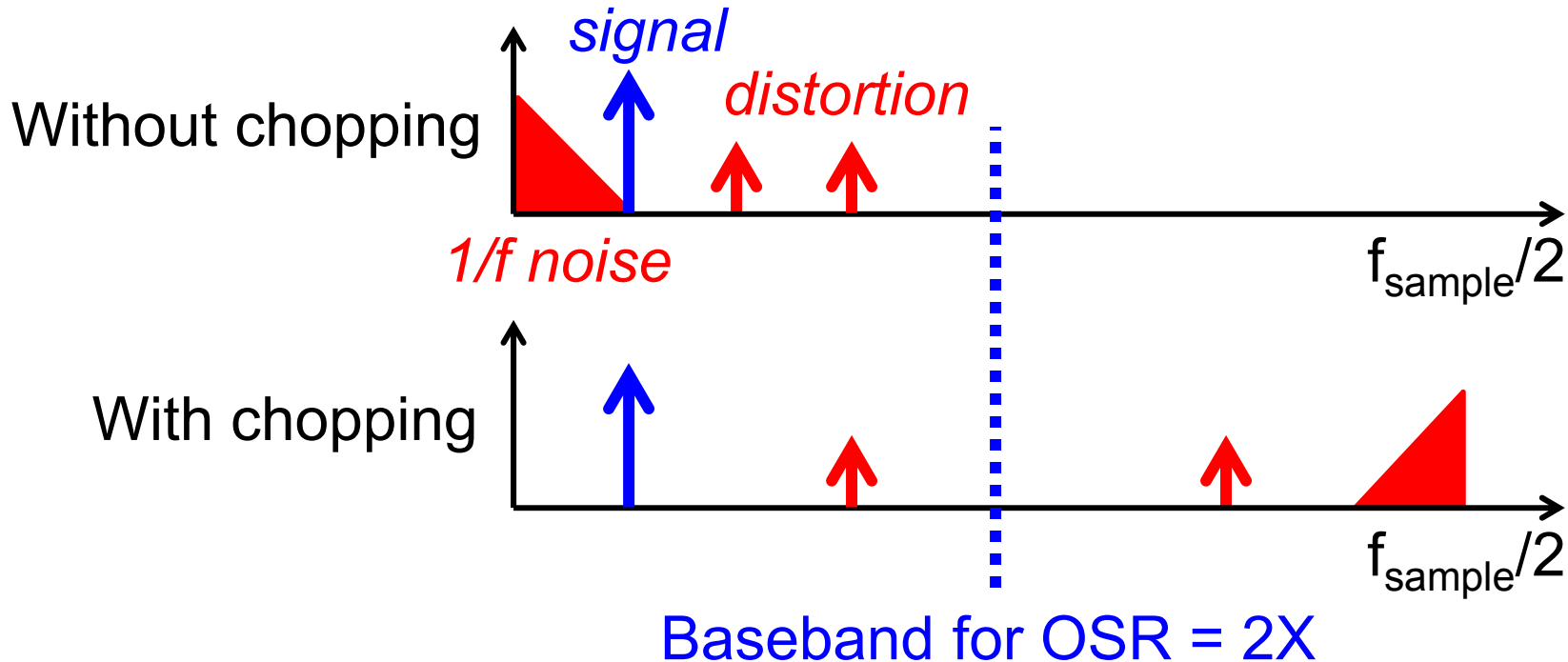
- Does not help for
 - $1/f$ noise
 - INL/DNL-induced distortion



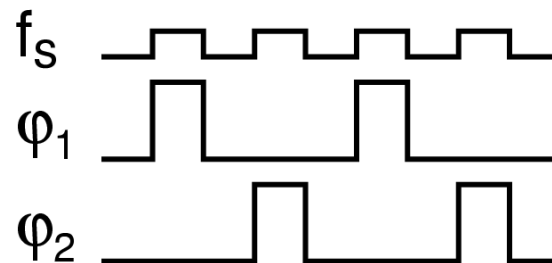
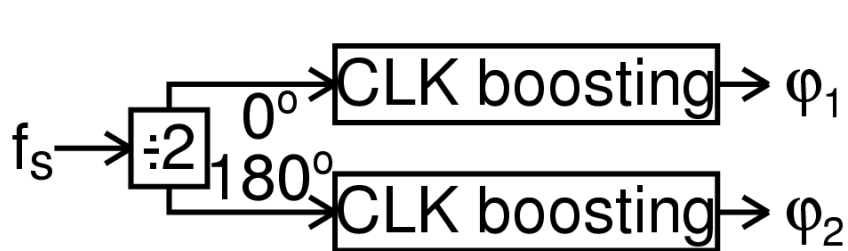
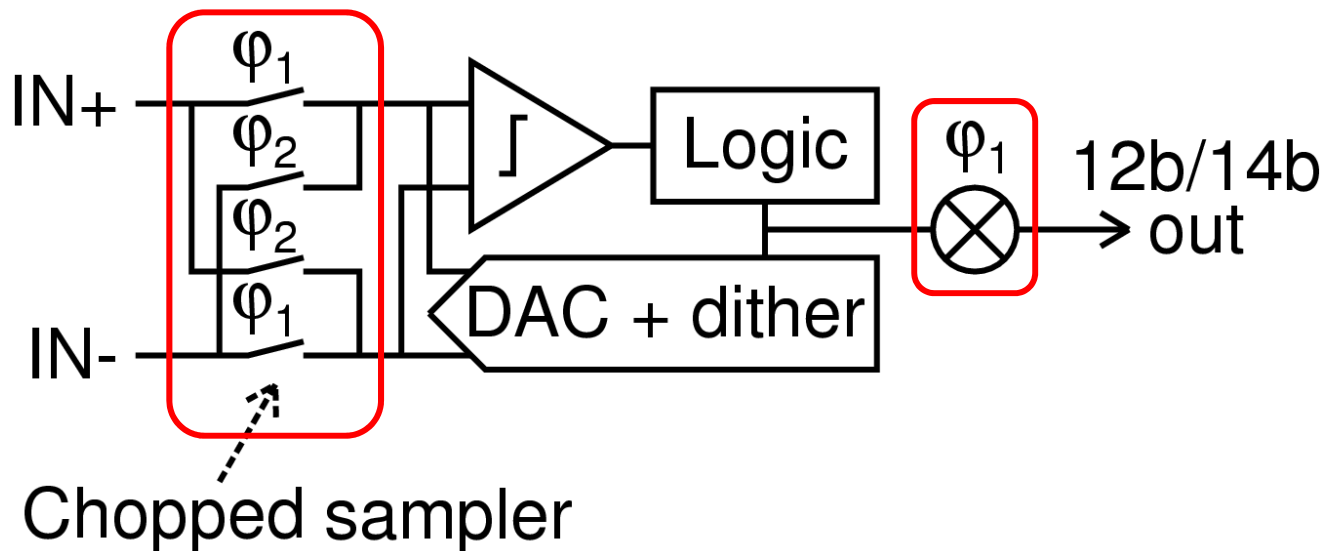
➔ Use chopping and dithering with oversampling

Chopping Principle

- $1/f$ noise and distortion modulated with f_{chop}
- $f_{\text{chop}} = \frac{1}{2} f_{\text{sample}}$ and $\text{OSR} \geq 2X \rightarrow$
 $1/f$ noise and even-order HD moved out of baseband



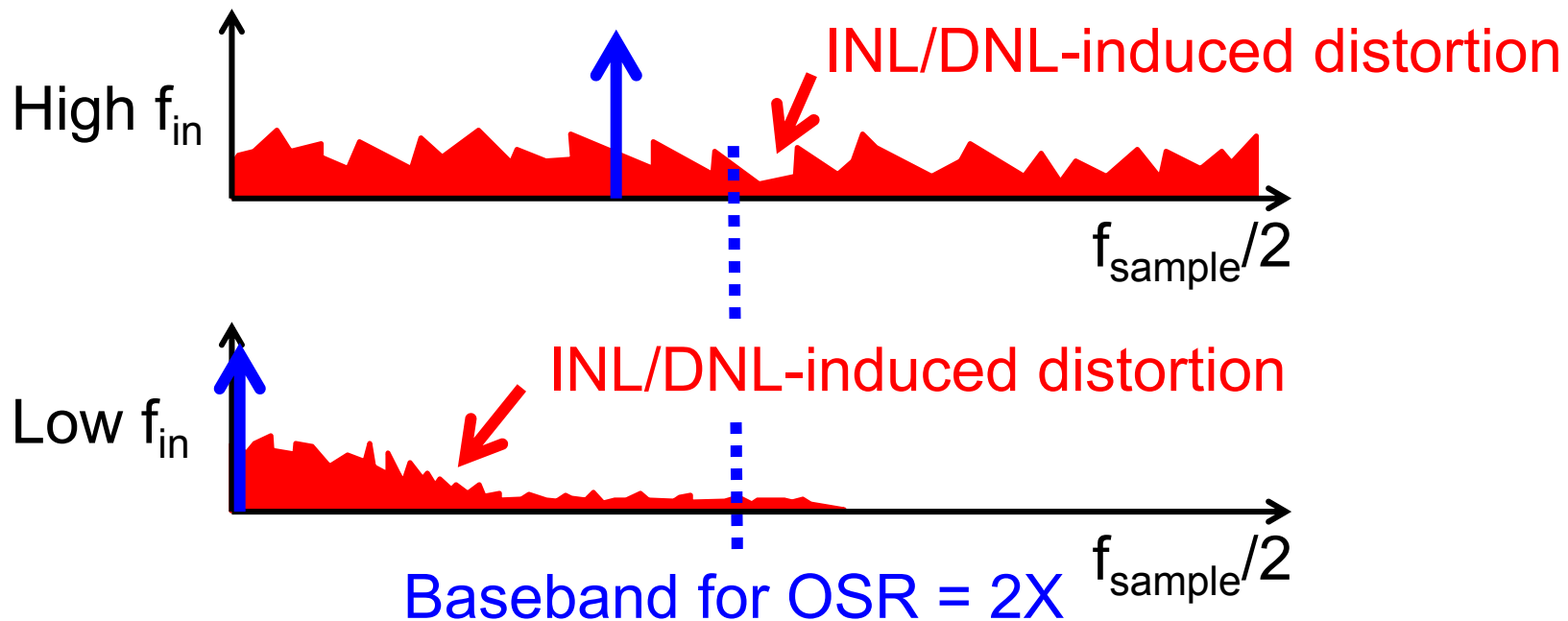
Chopping Implementation



- Negligible power/area overhead

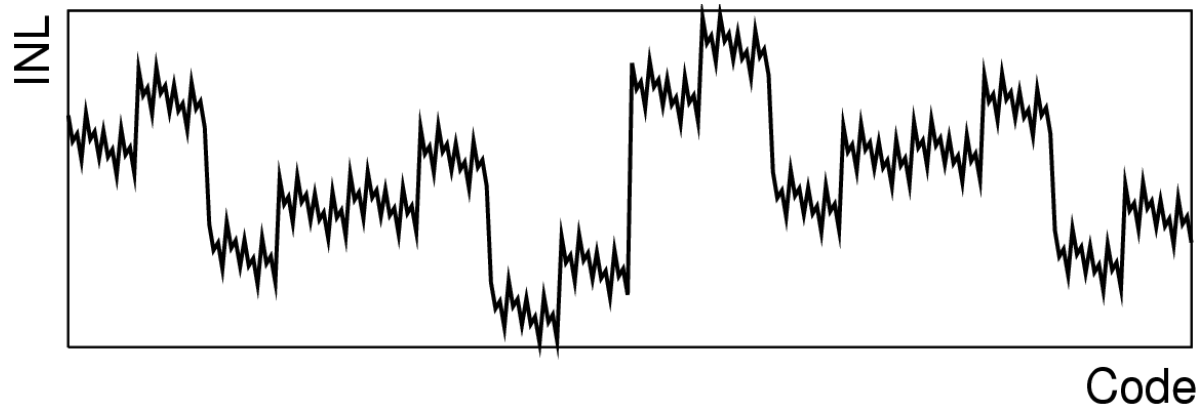
INL/DNL-Induced Distortion

- Limited DAC matching \rightarrow INL/DNL-induced distortion

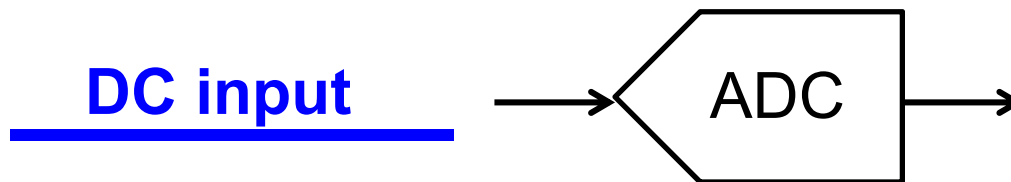
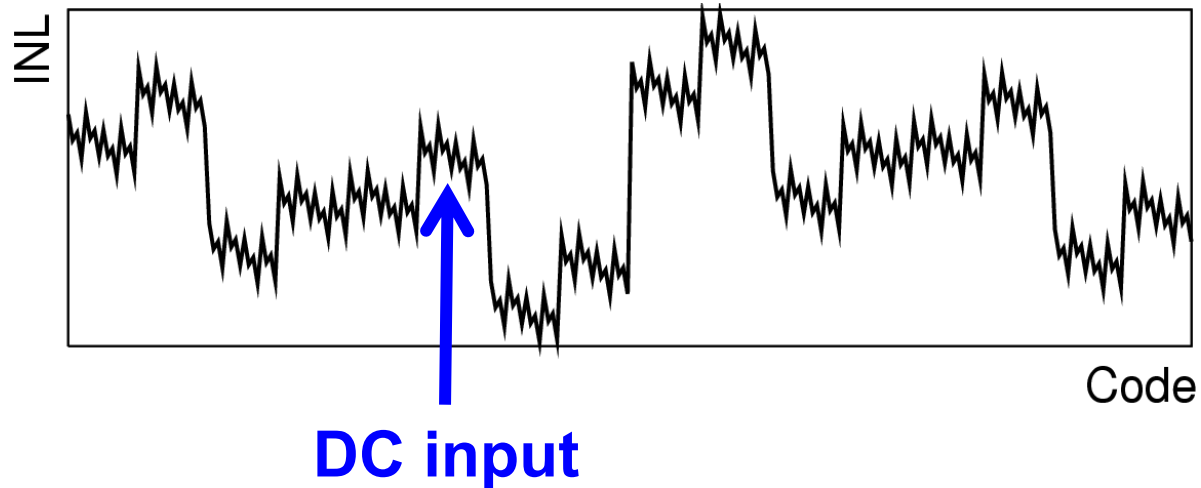


- Oversampling helps only for high f_{in} , not for low f_{in}
- Chopping helps only for even-order HD; not for odd

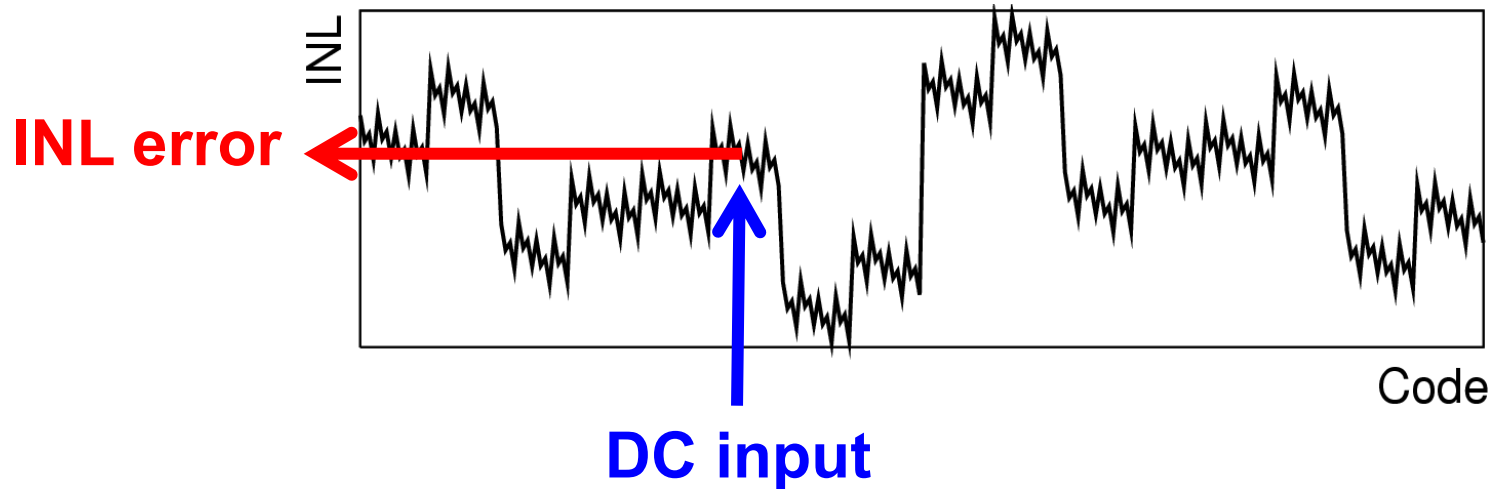
Dithering Principle – Example for DC



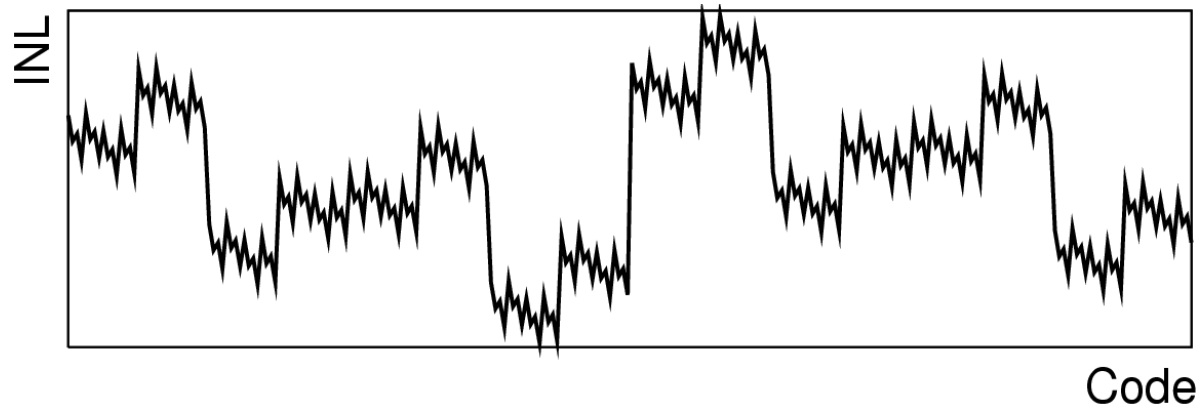
Dithering Principle – Example for DC



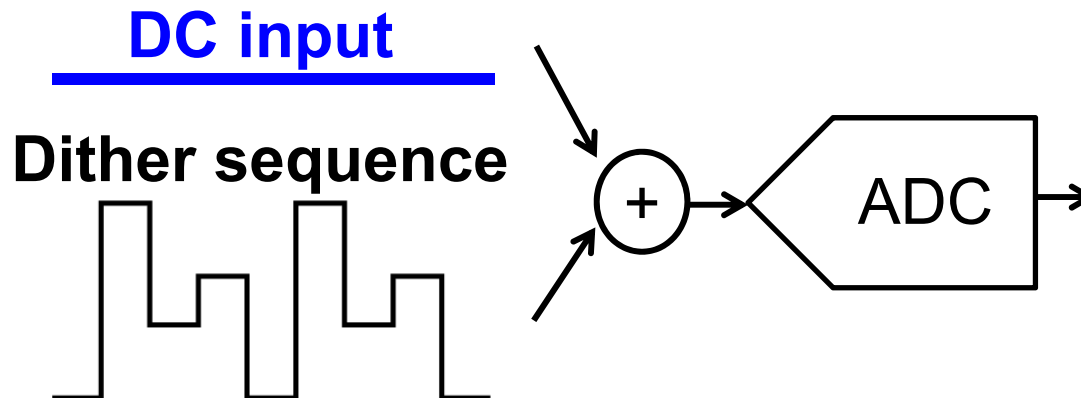
Dithering Principle – Example for DC



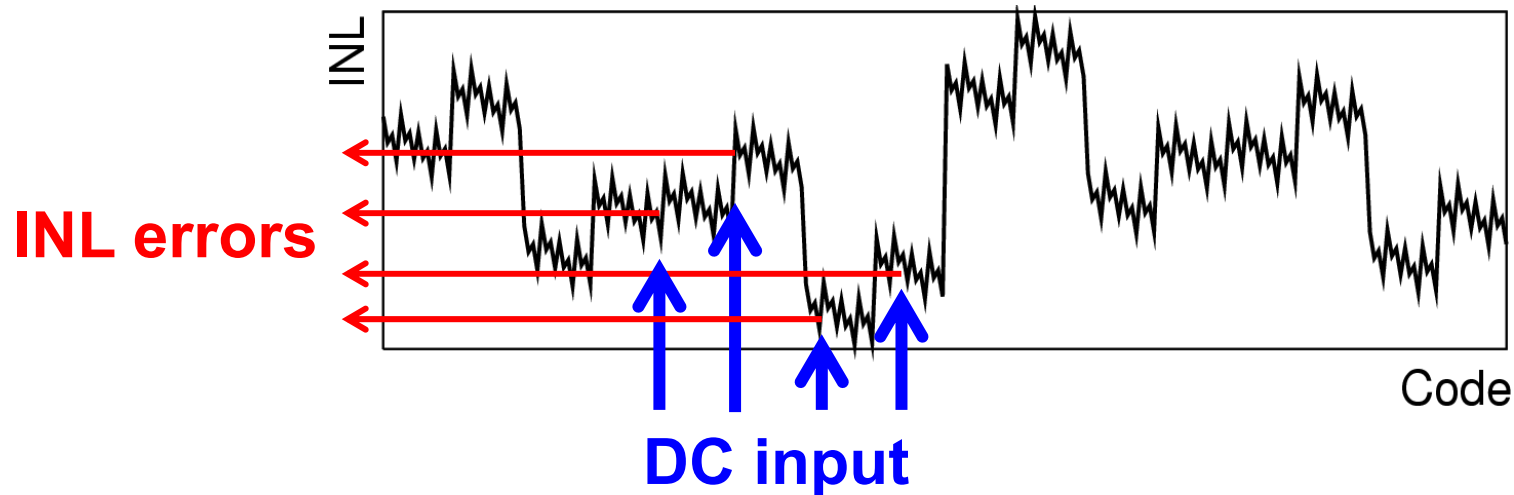
Dithering Principle – Example for DC



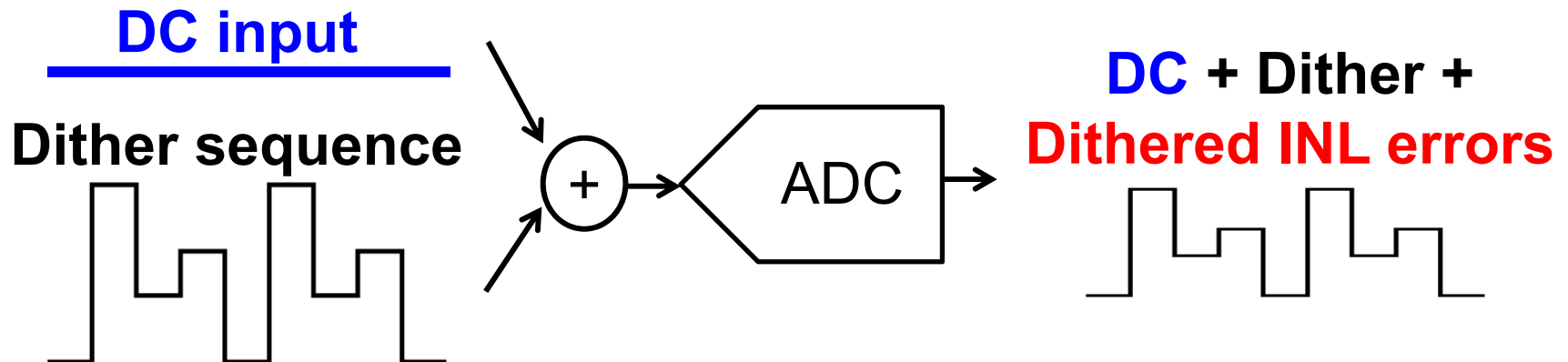
- Add deterministic dither before AD conversion



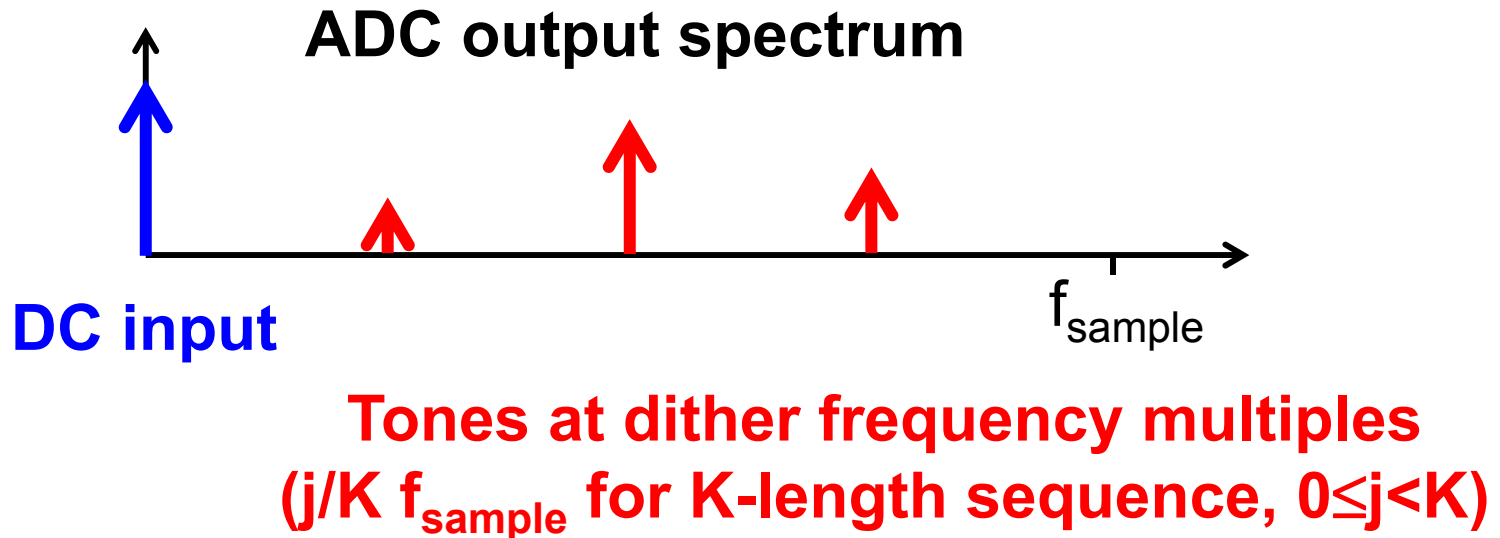
Dithering Principle – Example for DC



- Add deterministic dither before AD conversion

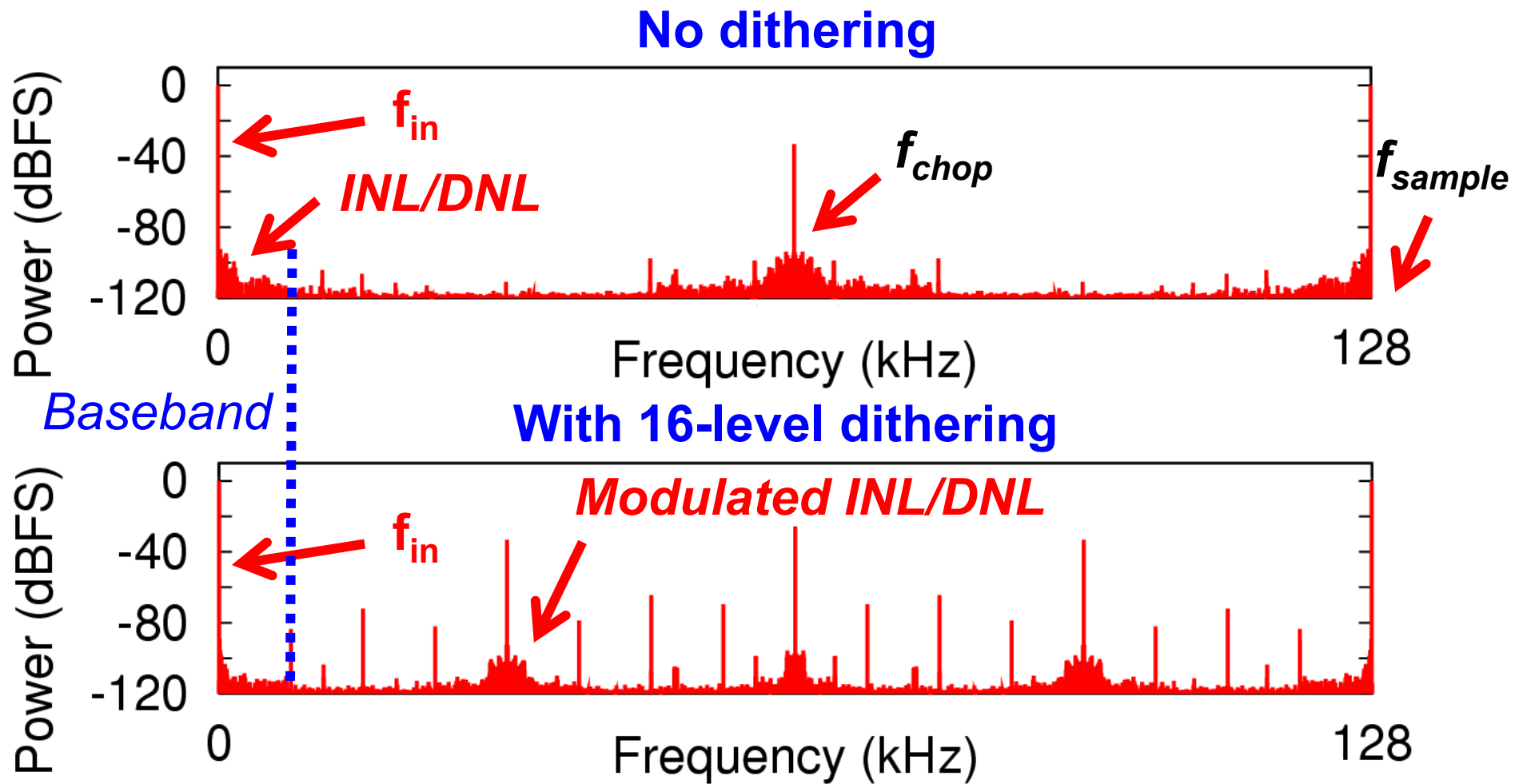


Dithering Principle – Example for DC

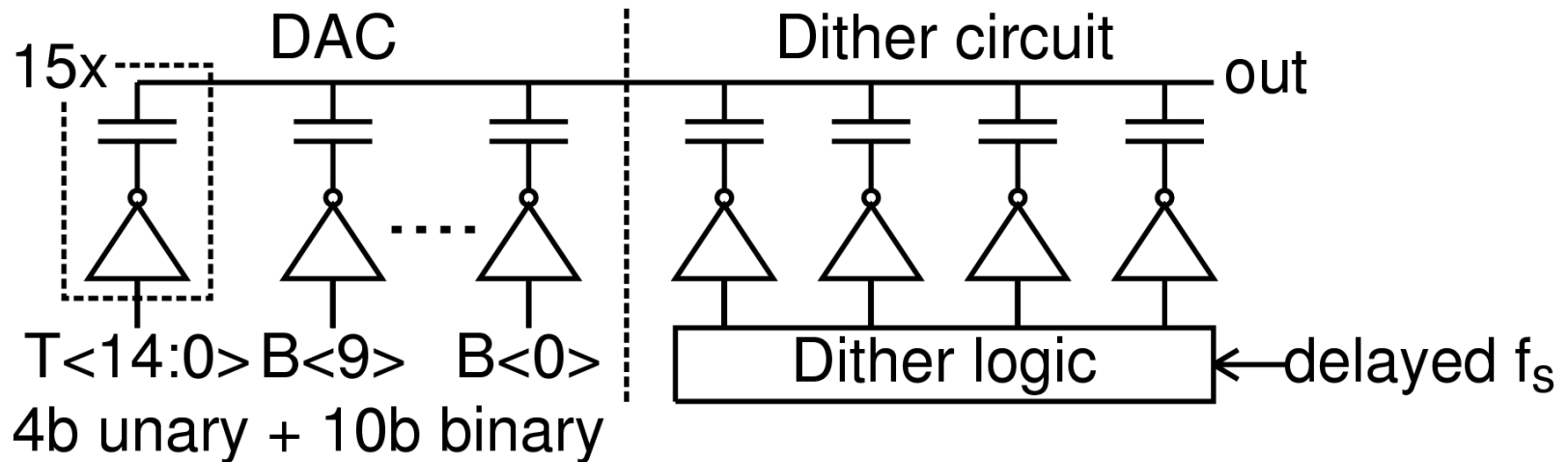


- Dithering modulates INL/DNL errors → averaging
 - Deterministic → Errors modulated to specific frequencies
 - With oversampling → Dither tones will be out-of-band
 - Non-subtractive → Dither tones outside band anyhow

Dithering - Example AC Measurement



Dithering Implementation

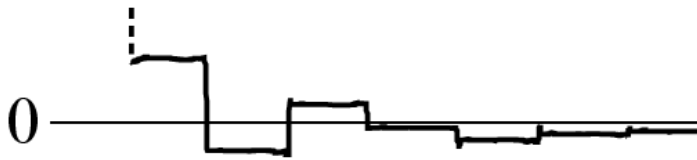


- Capacitive addition after sampling, before conversion
- 4 capacitors \rightarrow 16 possible dither levels
- Logic: counter at f_{sample} , creates 4 or 16 levels
- Total dither capacitance (and thus power and area) only 4% of DAC itself \rightarrow Efficient solution

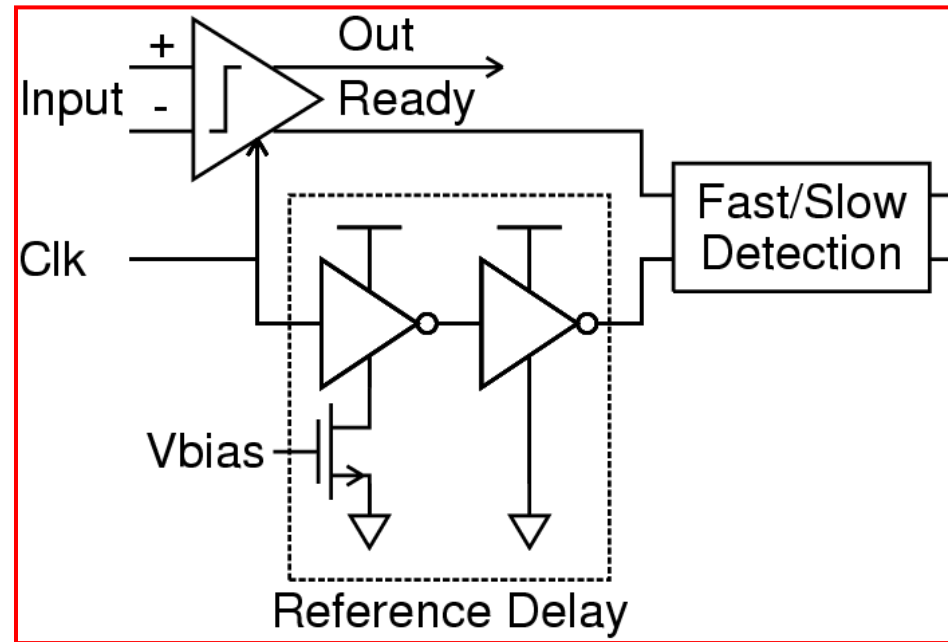
Data-Driven Noise Reduction (DDNR)

- Selective reduction of comparator noise using majority voting (*Harpe, et al, ISSCC 2013 [1]*)

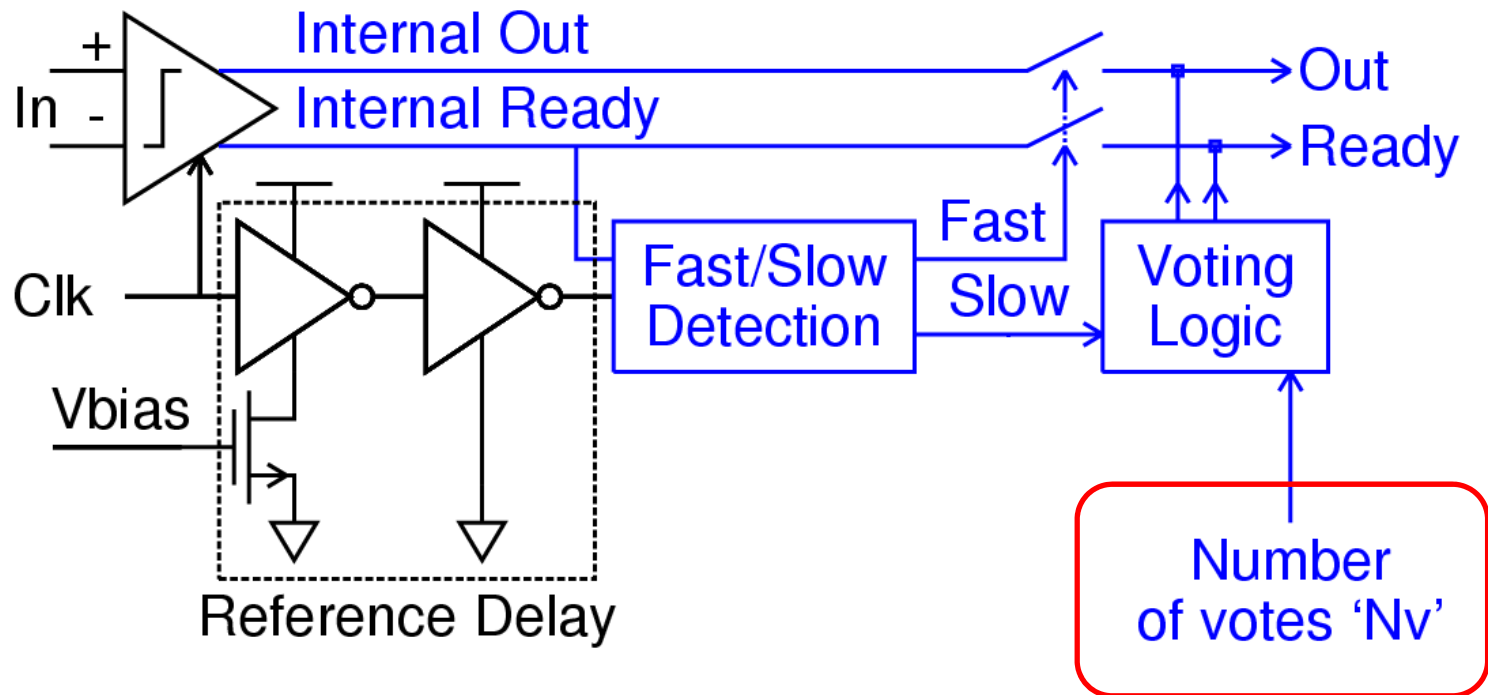
Comparator input
as function of time



- Noise reduction depends on:
 - N_v : number of votes
 - N_c : number of critical cycles per conversion
- Drawbacks in [1]: N_v fixed to 5, N_c manually tuned by V_{bias}



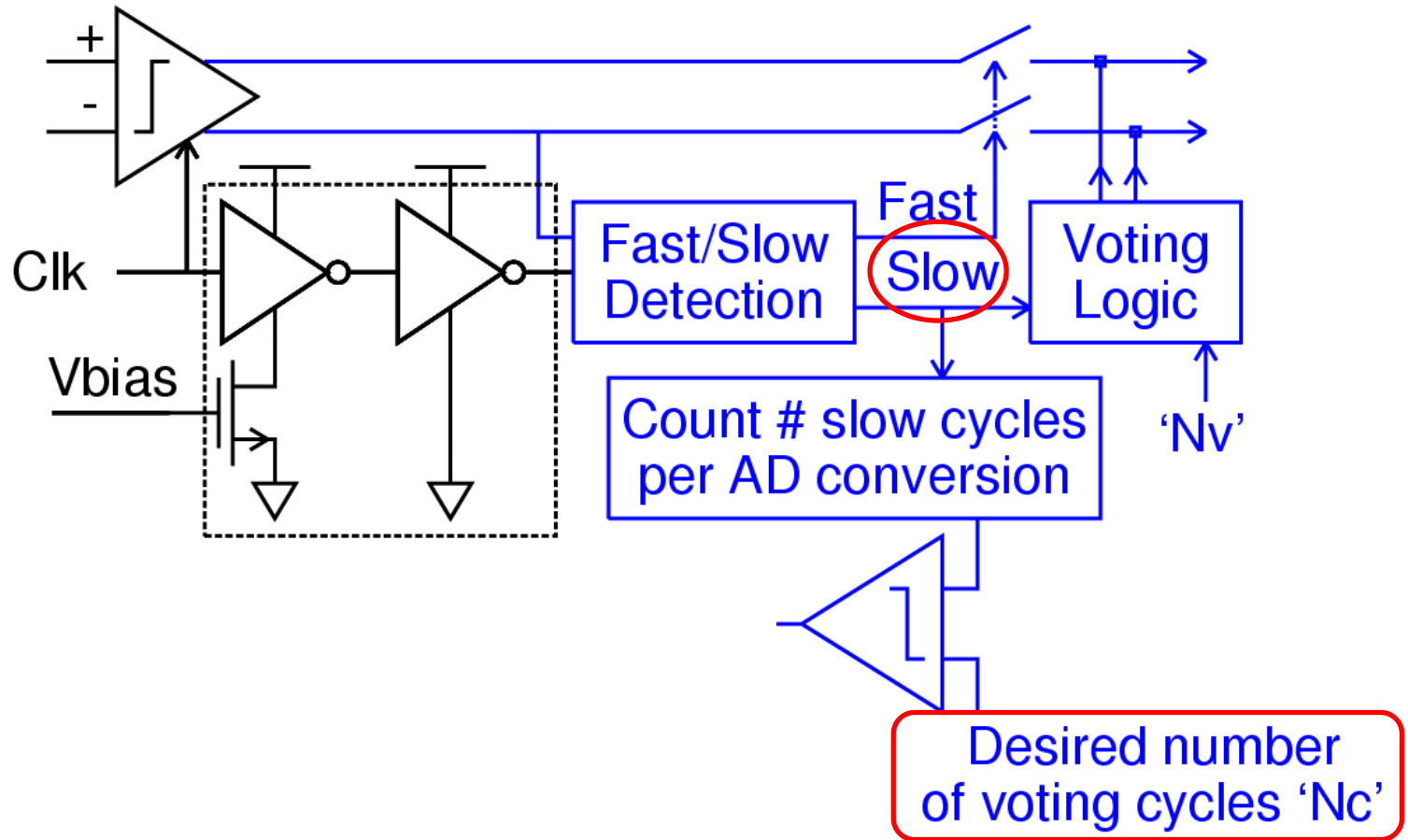
Feedback-Controlled DDNR



Analog

Digital

Feedback-Controlled DDNR

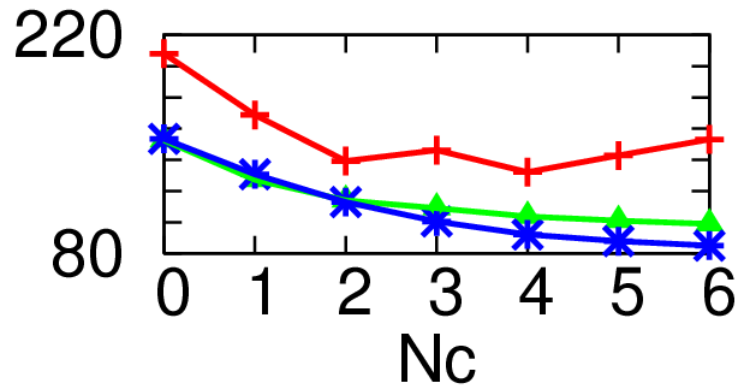


Analog

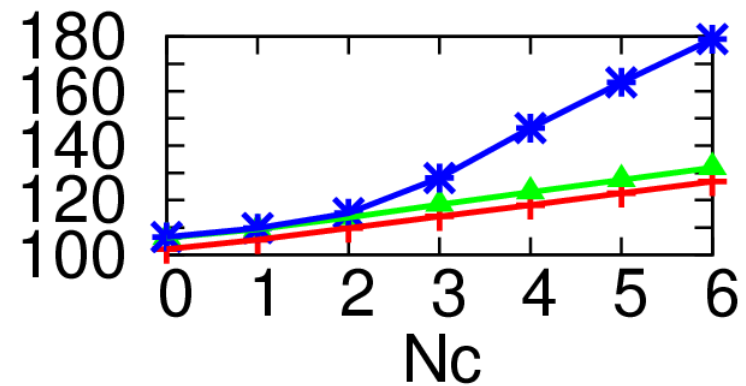
Digital

Measured Programmability of DDNR

ADC input-ref. Noise (μV_{rms})



ADC power @ 10kS/s (nW)



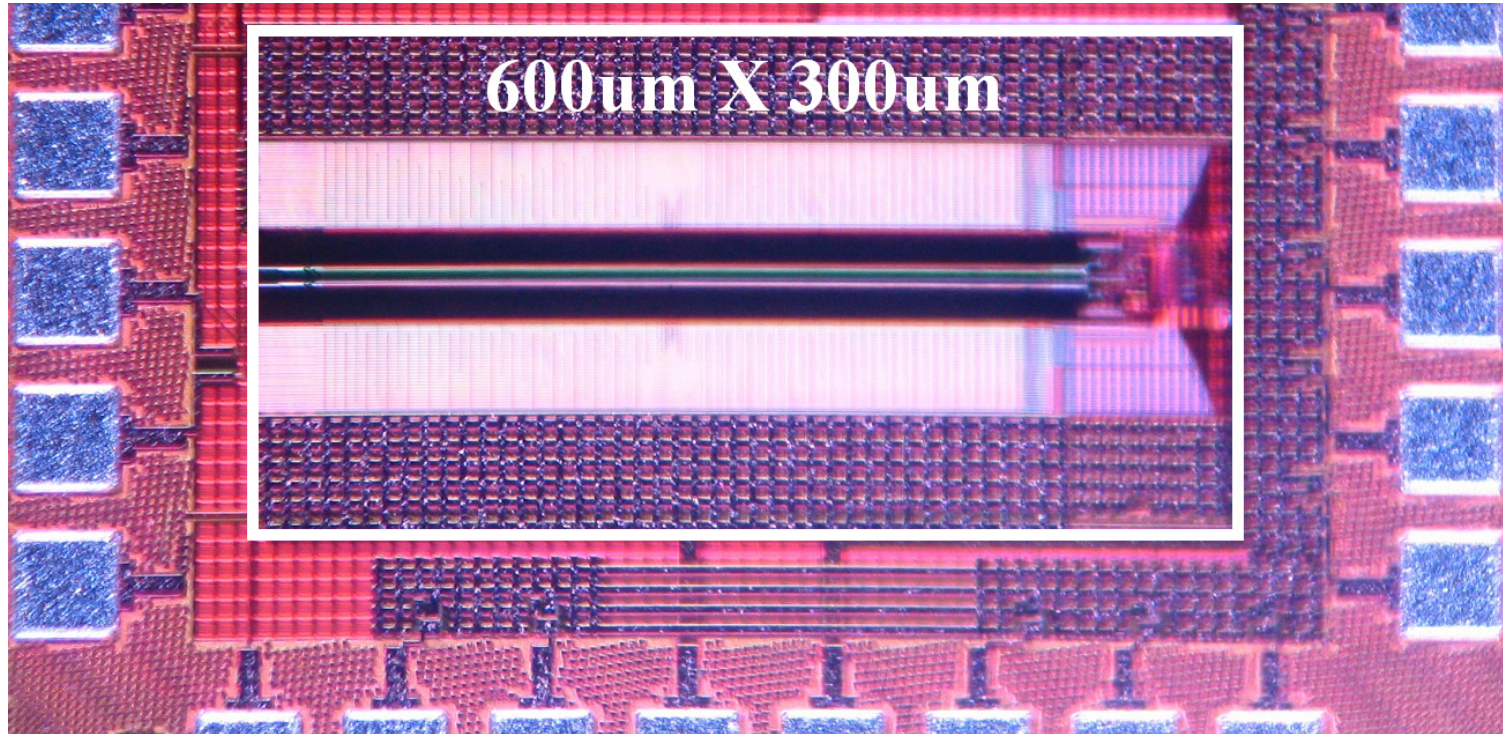
12b, $N_v = 5$ —+

14b, $N_v = 5$ —▲

14b, $N_v = 15$ —*

- Noise reduced as function of
 - N_v – Number of votes
 - N_c – Number of voting cycles
- Power-efficient and flexible noise reduction

Die Photo, 65nm CMOS

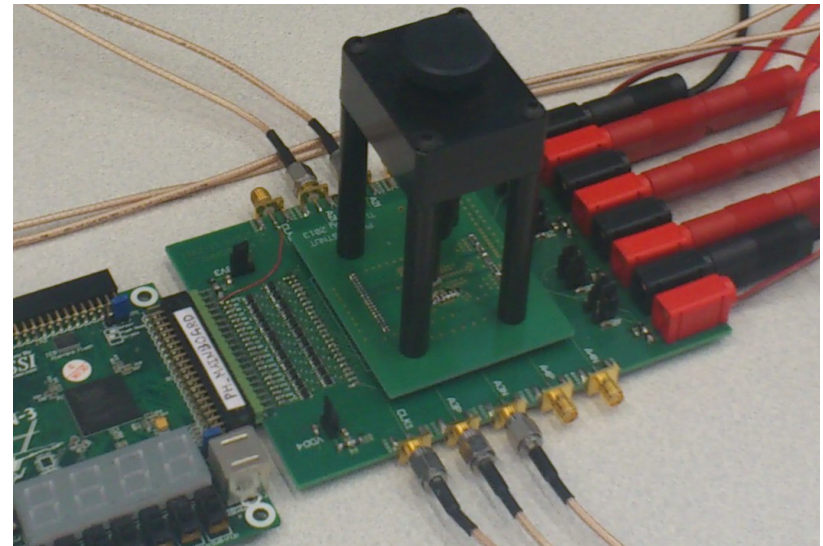


- Total area: 0.18mm^2
- Area includes supply/reference decoupling caps

Measured Modes of Operation

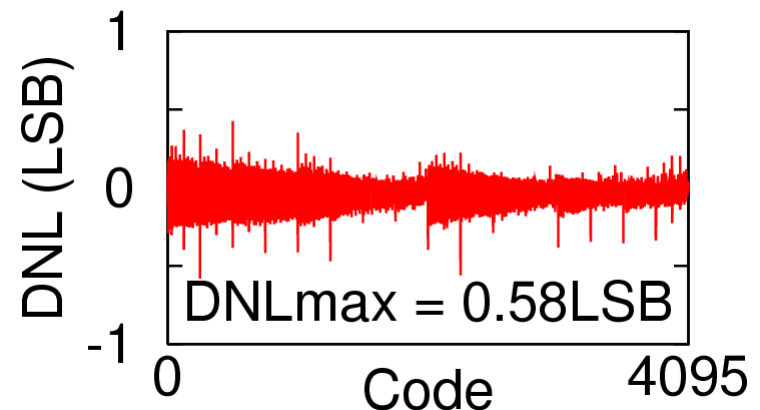
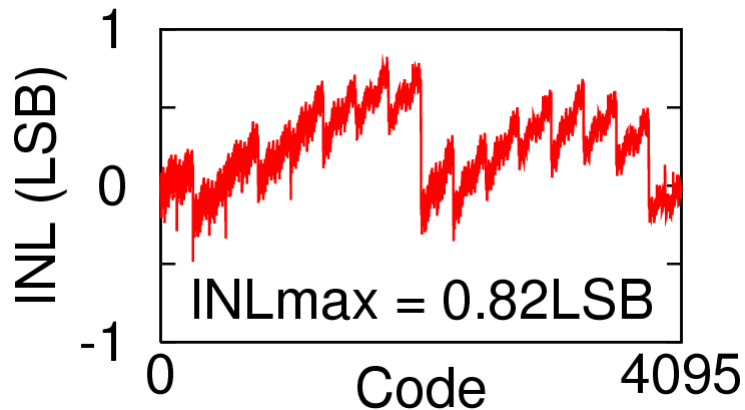
Mode	Enabled options
12b, 32kS/s – Nyquist	DDNR, $N_v = 5$, $N_c = 2$
14b, 32kS/s – Nyquist	DDNR, $N_v = 5$, $N_c = 4$
14b, 128kS/s, 4X OSR	DDNR, chopping and 4-level dithering
14b, 128kS/s, 16X OSR	DDNR, chopping and 16-level dithering

- All at 0.8V supply

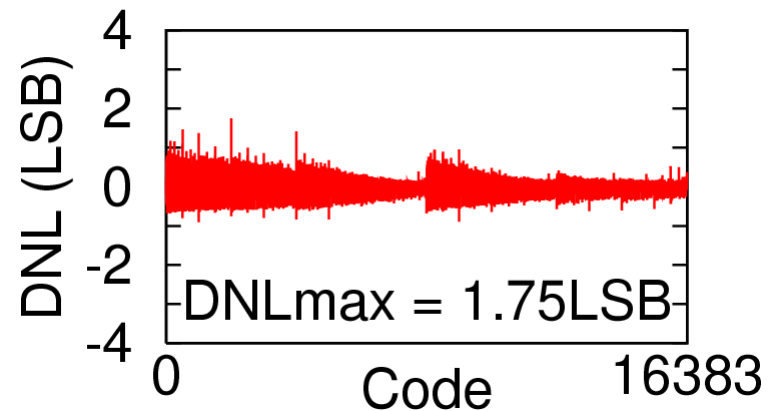
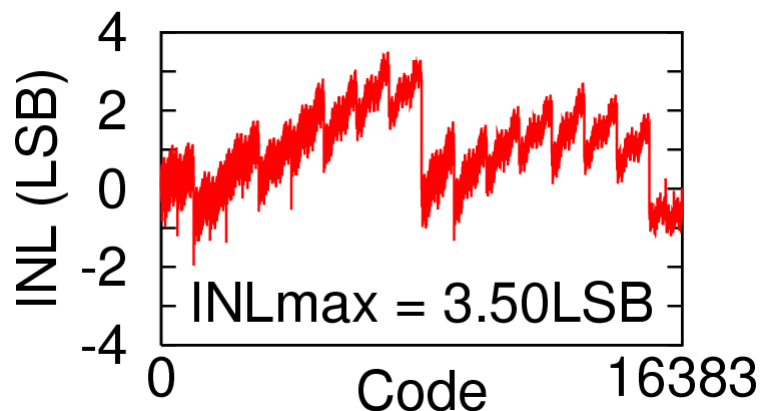


Measured INL/DNL – Nyquist Modes

12bit mode



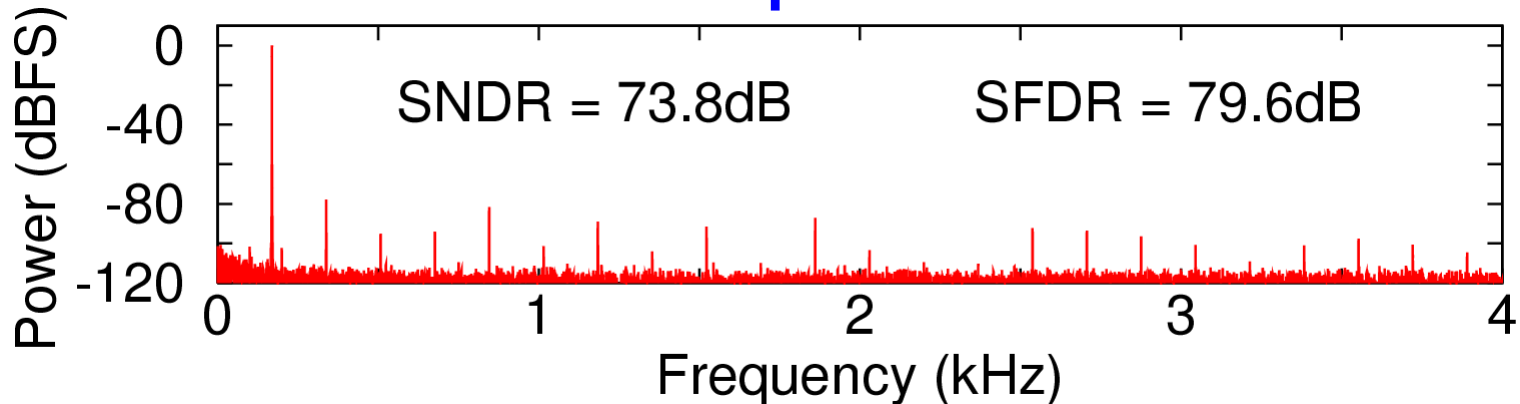
14bit mode



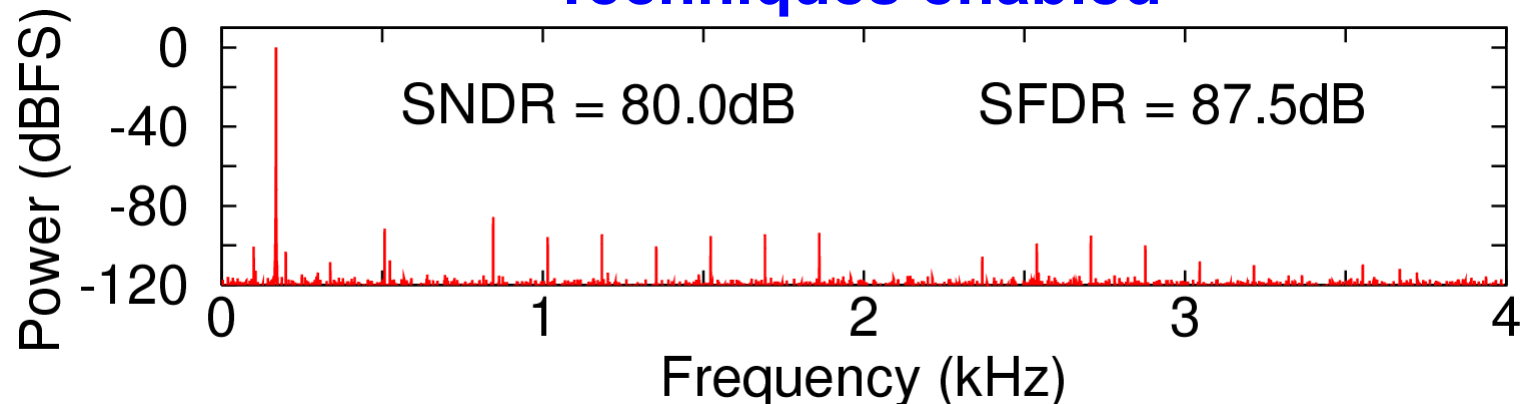
Effect of Chopping, Dithering and DDNR

- 14b mode, 128kS/s, 16X OSR, $f_{in} = 169.22\text{Hz}$

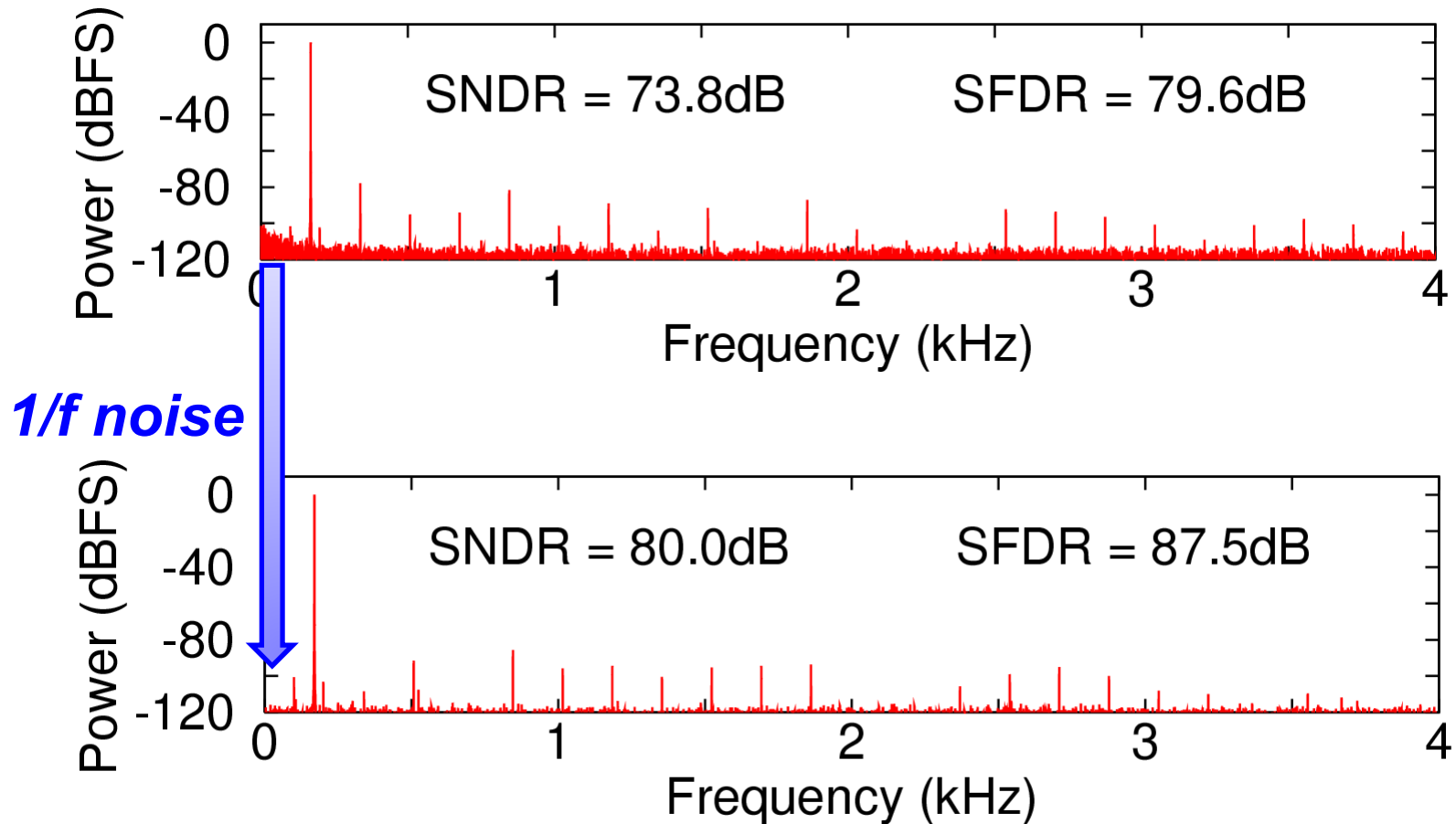
Techniques disabled



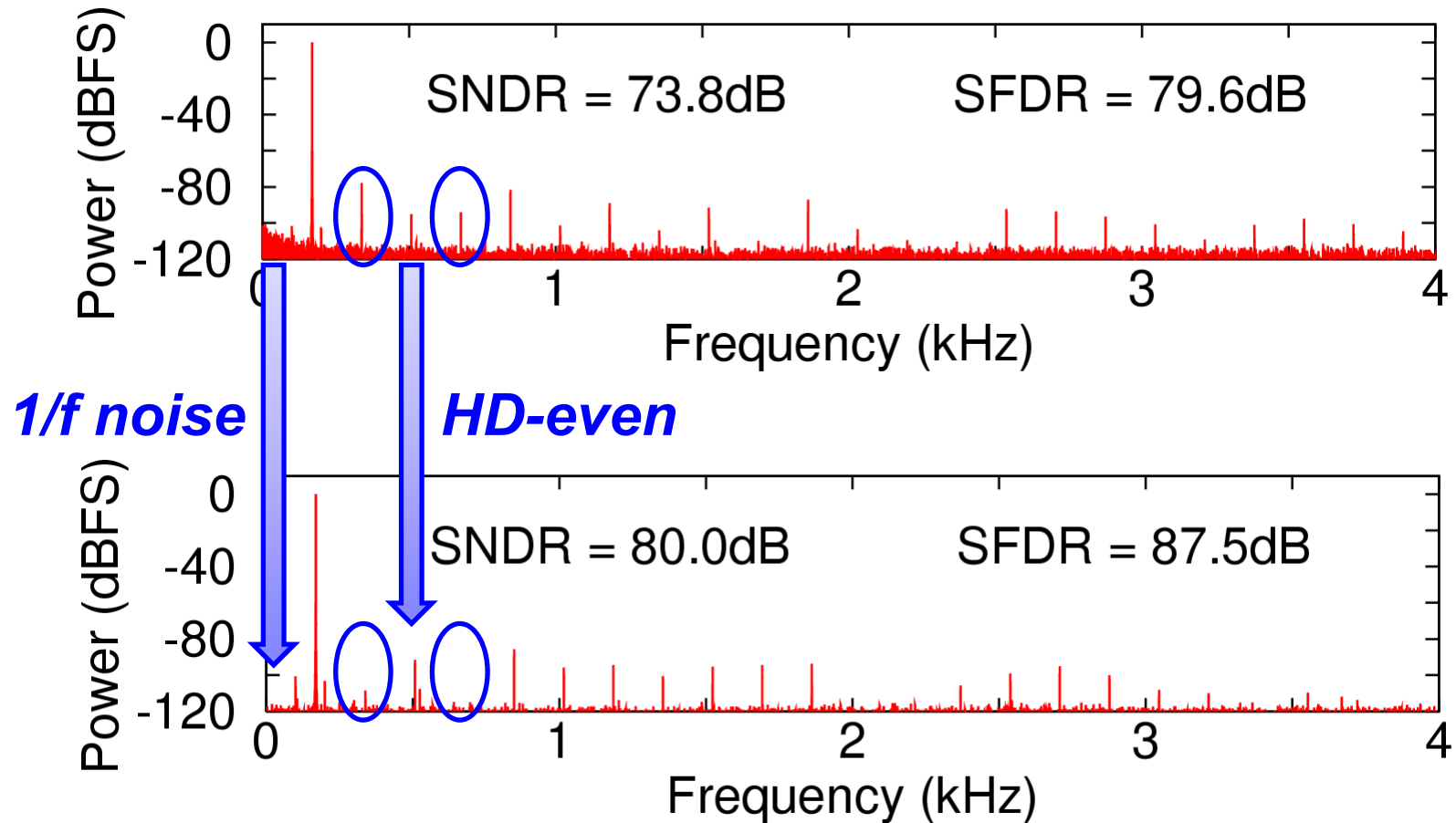
Techniques enabled



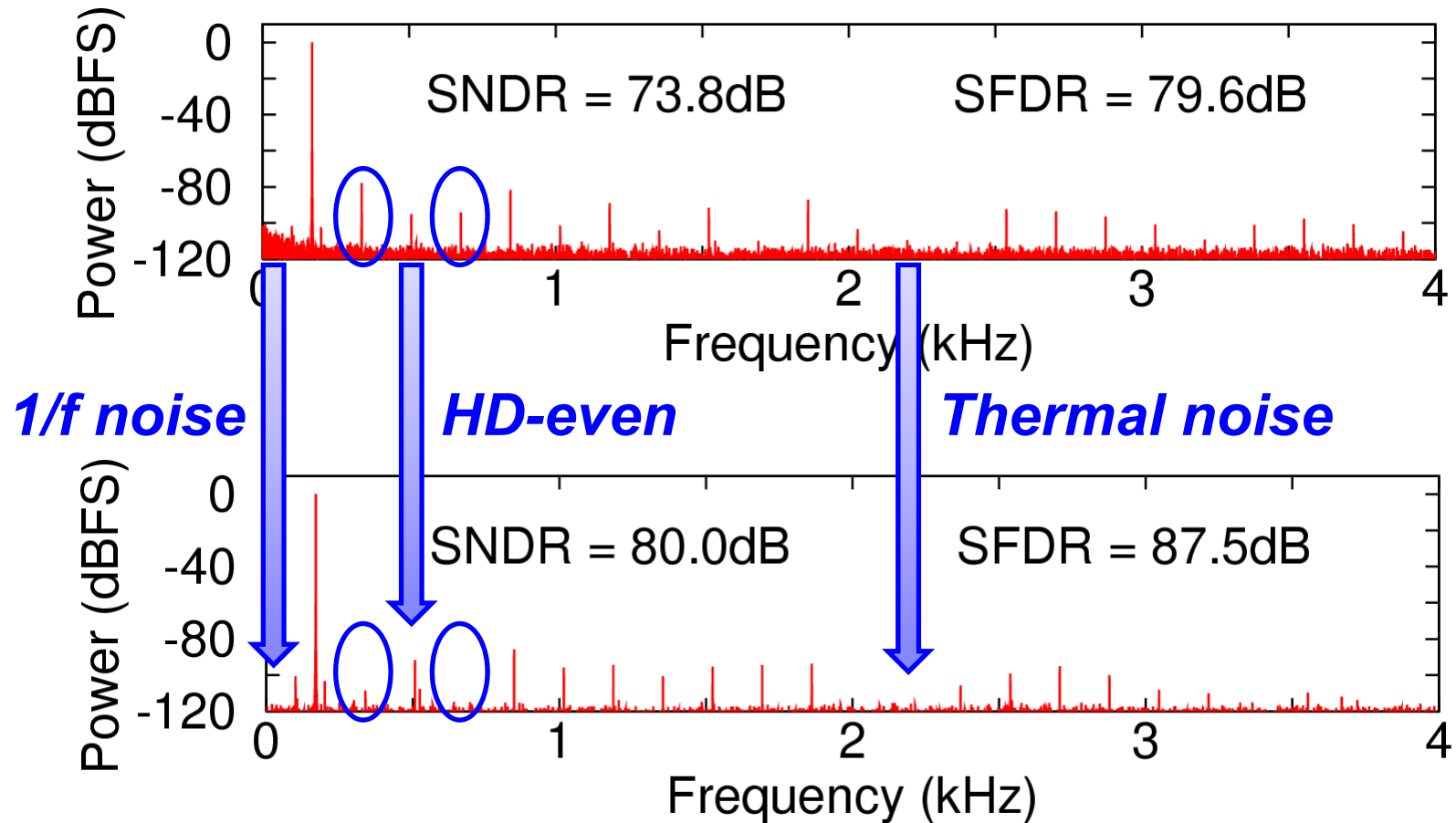
Effect of Chopping, Dithering and DDNR



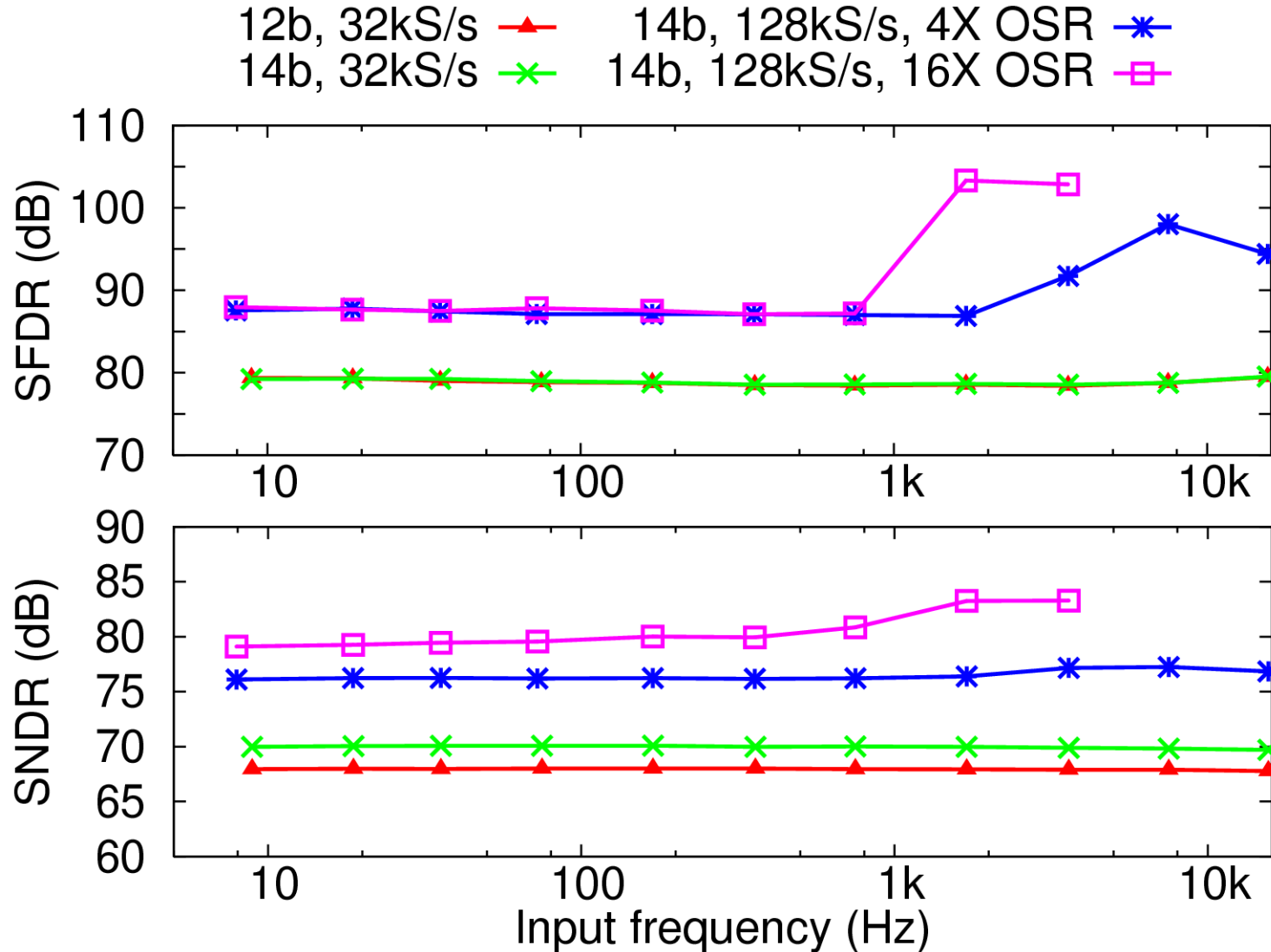
Effect of Chopping, Dithering and DDNR



Effect of Chopping, Dithering and DDNR

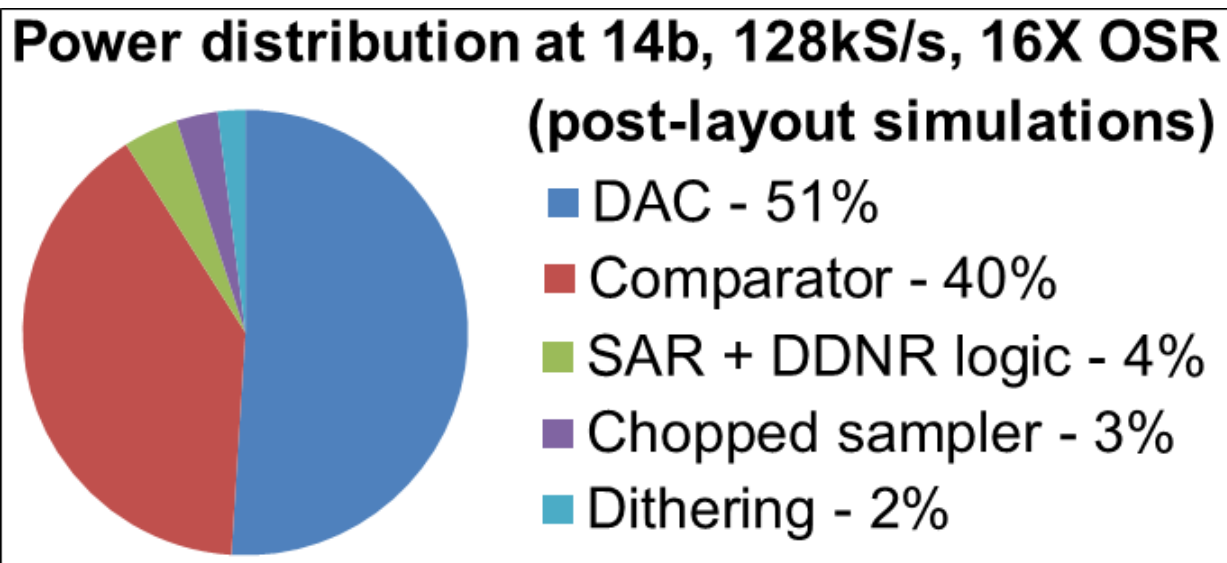


SFDR and SNDR versus f_{in}



Measured Power Consumption

Mode	Power
12b, 32kS/s	0.310 μ W
14b, 32kS/s	0.352 μ W
14b, 128kS/s, 4X OSR	1.367 μ W
14b, 128kS/s, 16X OSR	1.370 μ W



- Chopping and dithering add negligible overhead

ADC Performance Summary

	[1]	[2]	[3]	This work			
Architecture	SAR	SAR	$\Sigma\Delta$	SAR			
Resolution (bit)	12	10	-	12	14	14	14
Sample rate (kS/s)	40	500	3200	32	32	128	128
Oversampling ratio	-	-	16	-	-	4x	16x
Bandwidth (kHz)	20	250	100	16	16	16	4
#votes N_v , #cycles N_c	5, -	-	-	5, 2	5, 4	5, 4	5, 4
Chopping	-	-	-	Off	Off	On	On
Dithering	-	-	-	Off	Off	4-level	16-level
Power (μ W)	0.097	0.5	140	0.310	0.352	1.367	1.370
SFDR (dB)	68.8	81.3	96.0	78.4 *	78.5 *	86.9 *	87.1 *
SNDR (dB)	62.5	54.3	84.0	67.8 *	69.7 *	76.1 *	79.1 *
FOMW (fJ/conv.step)	2.2	2.4	54.0	4.8 *	4.4 *	8.2 *	23.2 *
FOMS (dB)	175.7	171.3	172.5	174.9 *	176.3 *	176.8 *	173.8 *

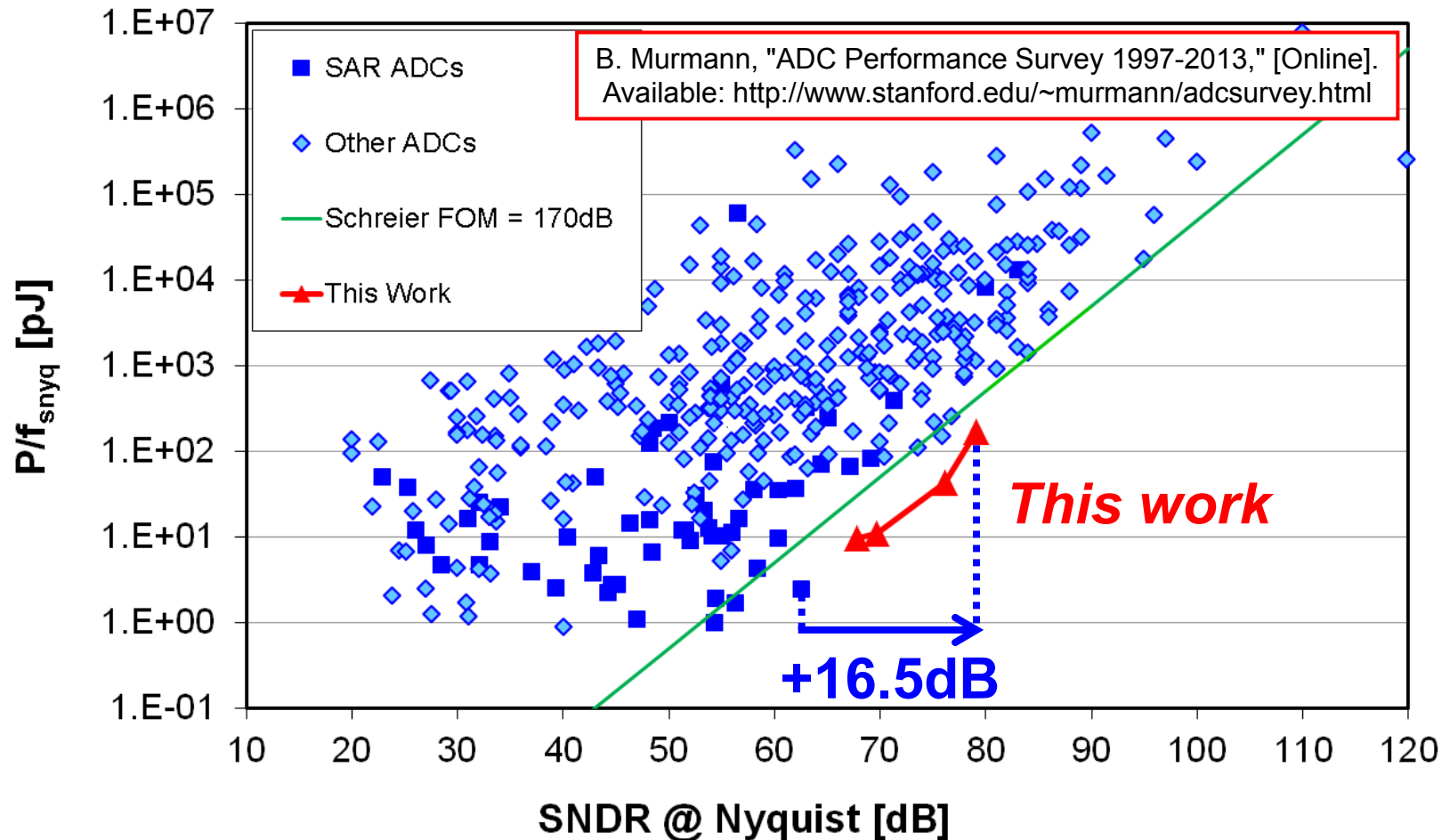
* Worst value across entire bandwidth

[1] Harpe, ISSCC2013

[2] Liou, ISSCC2013

[3] Perez, ISSCC2011

ADC Performance Comparison



- Extends SAR to higher ENOB with excellent FOM

Conclusions

- 12/14b SAR ADC
- Oversampling, Chopping and Dithering
 - Efficient suppression of noise and distortion
 - High SNDR without area/calibration penalty
- Feedback-Controlled Data-Driven Noise Reduction
 - Power-efficient SNR improvement
- Extends SAR application range to 79.1dB SNDR
- State-of-the-art FOM @ all resolutions

A 0.85fJ/conversion-step 10b 200kS/s Subranging SAR ADC in 40nm CMOS

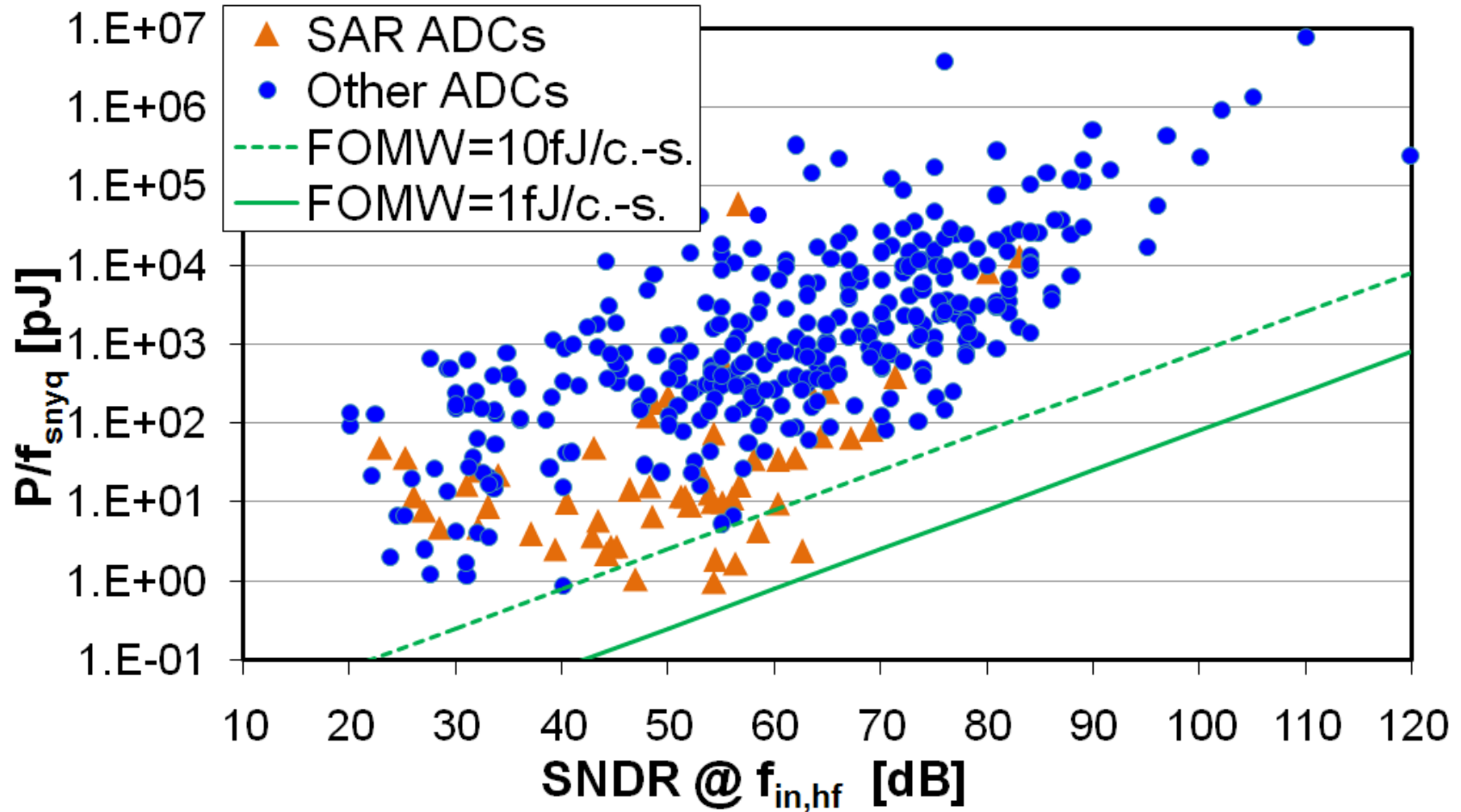
Hung-Yen Tai, Yao-Sheng Hu,
Hung-Wei Chen, and Hsin-Shu Chen

Graduate Institute of Electronics Engineering
National Taiwan University

Outline

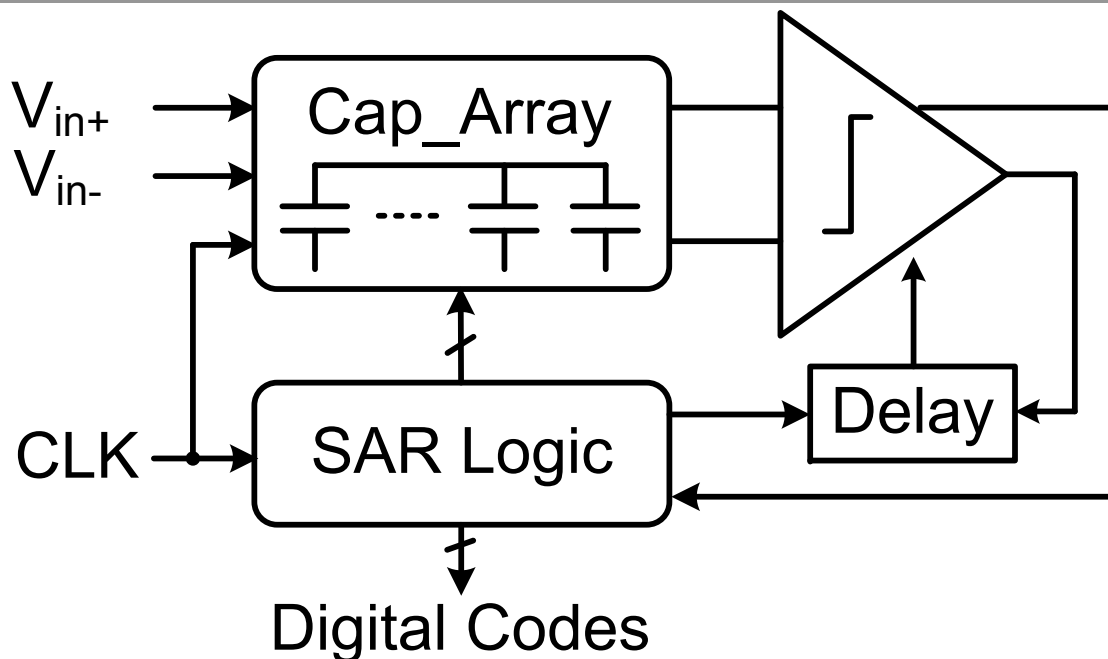
- Motivation
- Subranging SAR ADC Architecture
- Skipping Control Logic
 - Detect-and-Skip Algorithm
 - Aligned Switching Technique
- Comparator
- Measurement Results
- Conclusion

Motivation



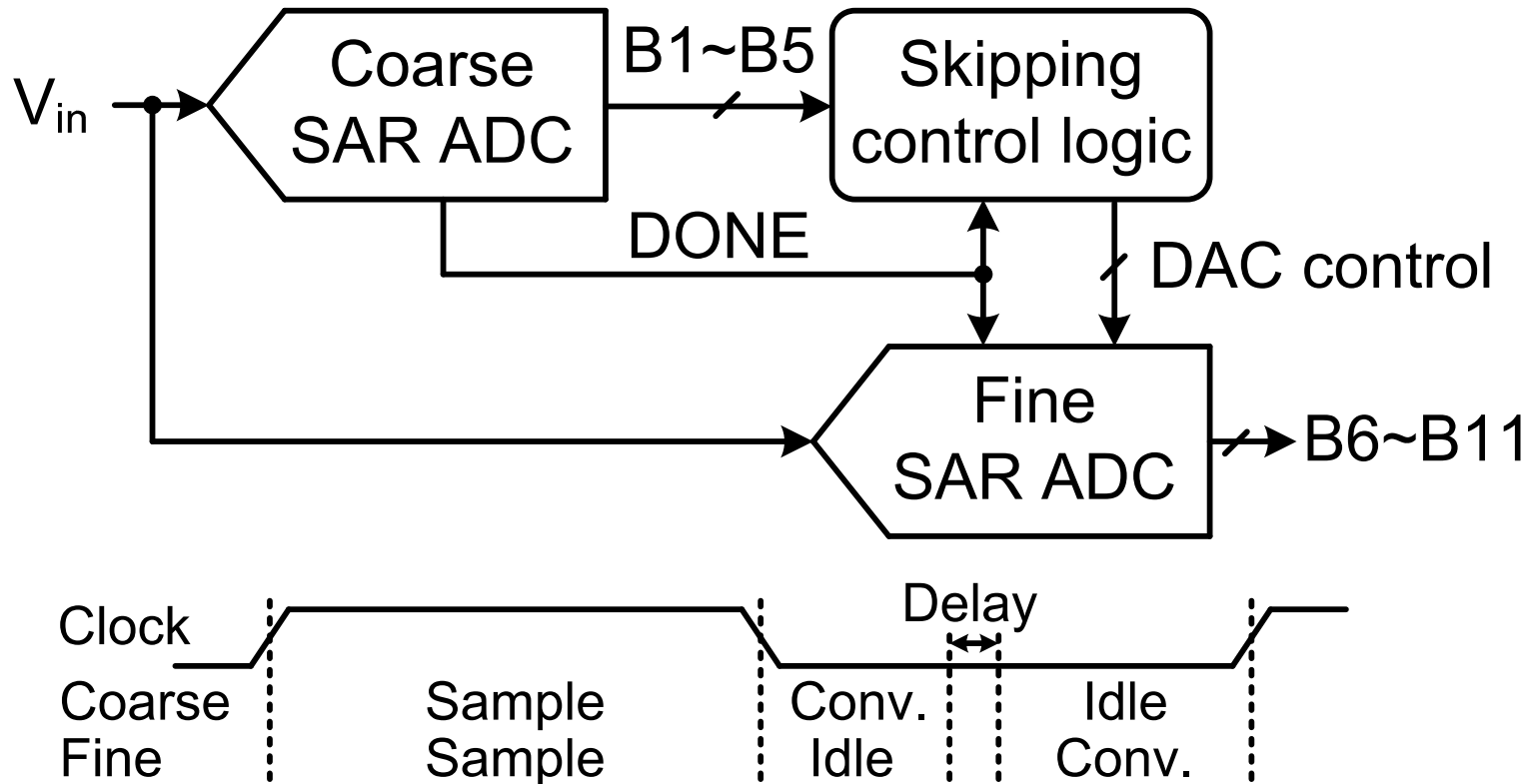
- B. Murmann, "ADC Performance Survey 1997-2013. "
<http://www.stanford.edu/~murmann/adcsurvey.html>.

Conventional Asynchronous SAR ADC



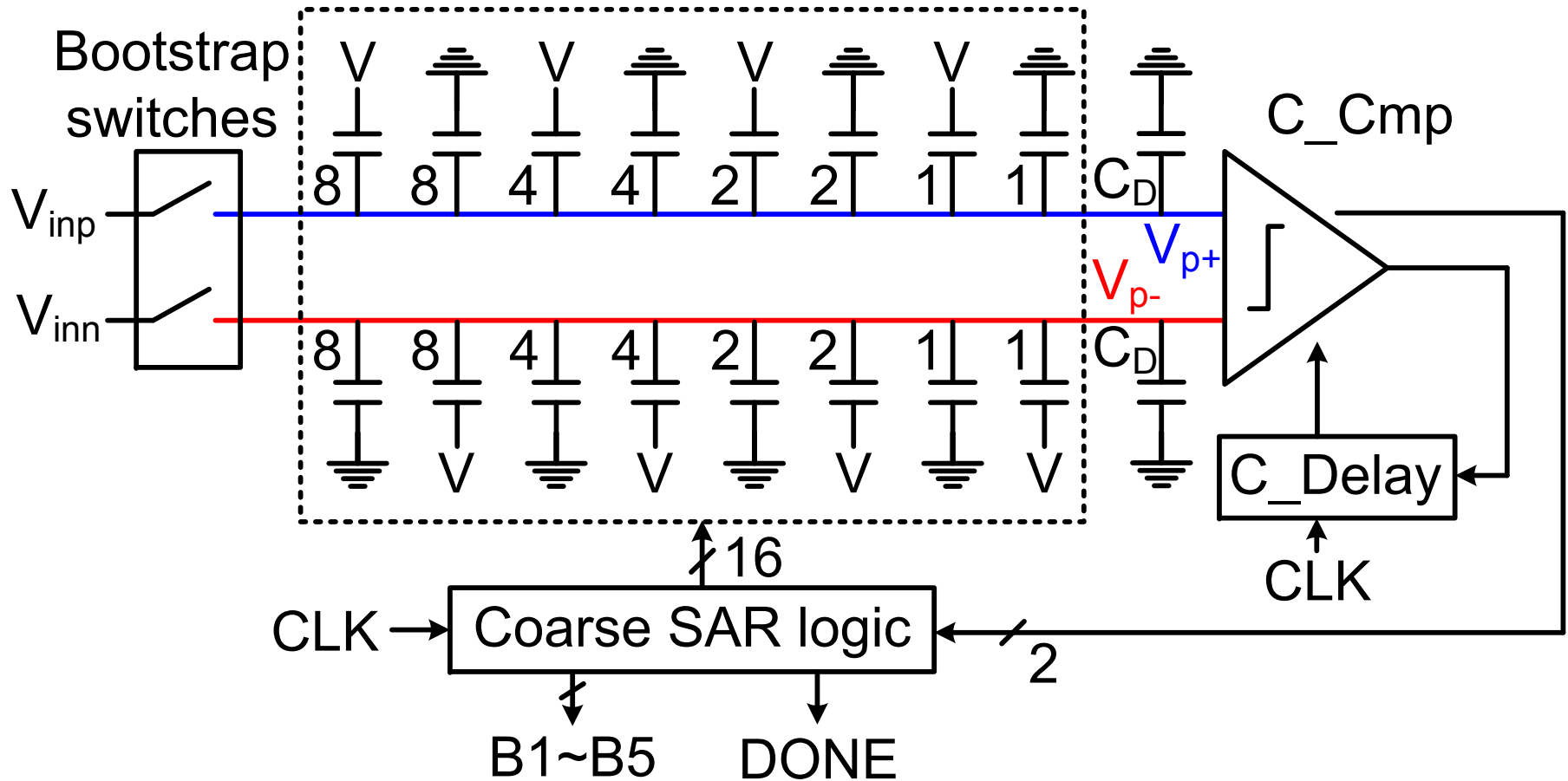
	Low resolution	High resolution
DAC size	Small	Large
Delay	Short	Long
Comparator	Low power	Low noise

Subranging SAR ADC Architecture



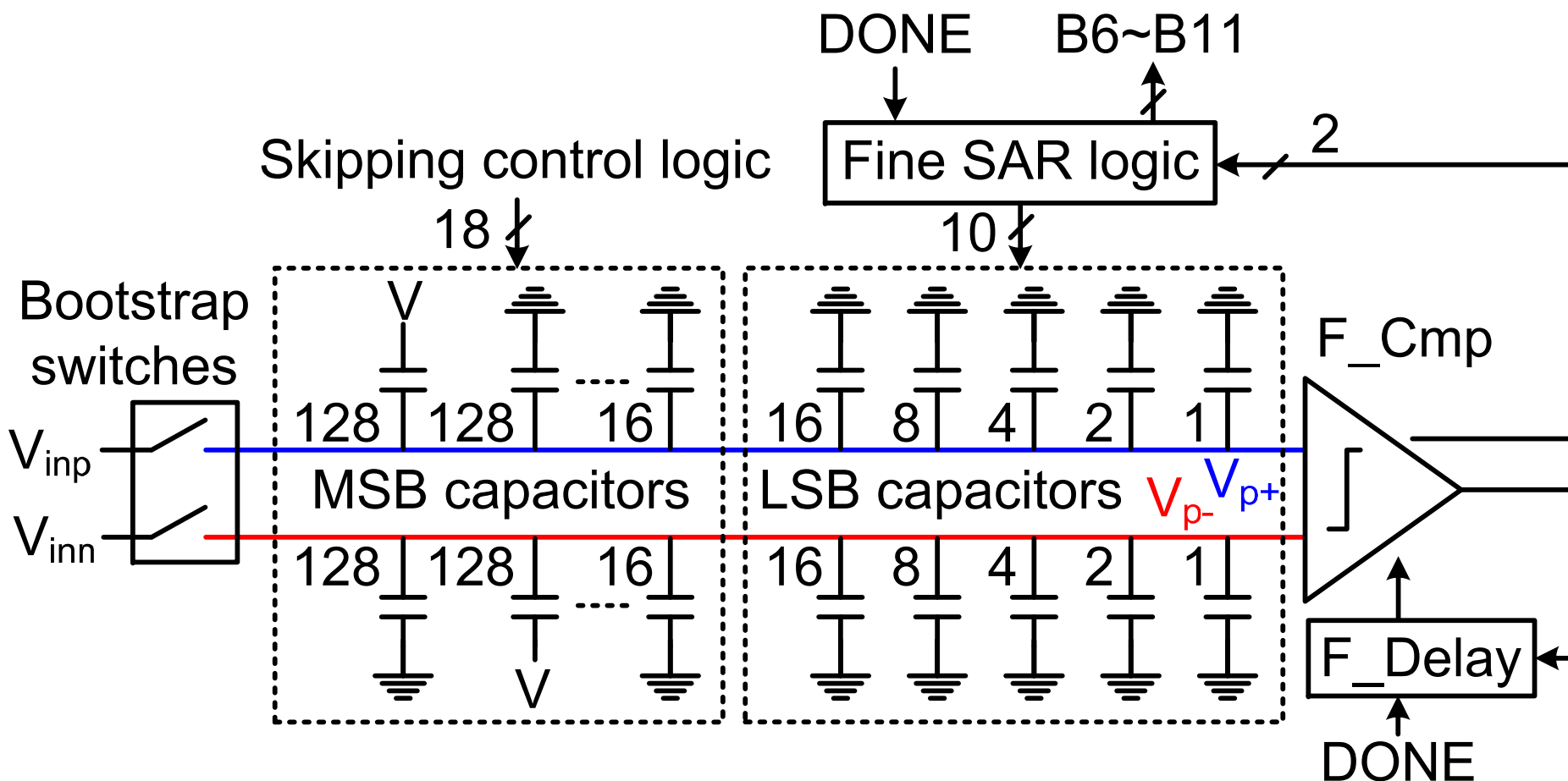
- Coarse ADC reduces Fine ADC power
- Skipping control logic saves Fine DAC power
 - Detect-and-Skip algorithm & Aligned switching technique

Coarse SAR ADC



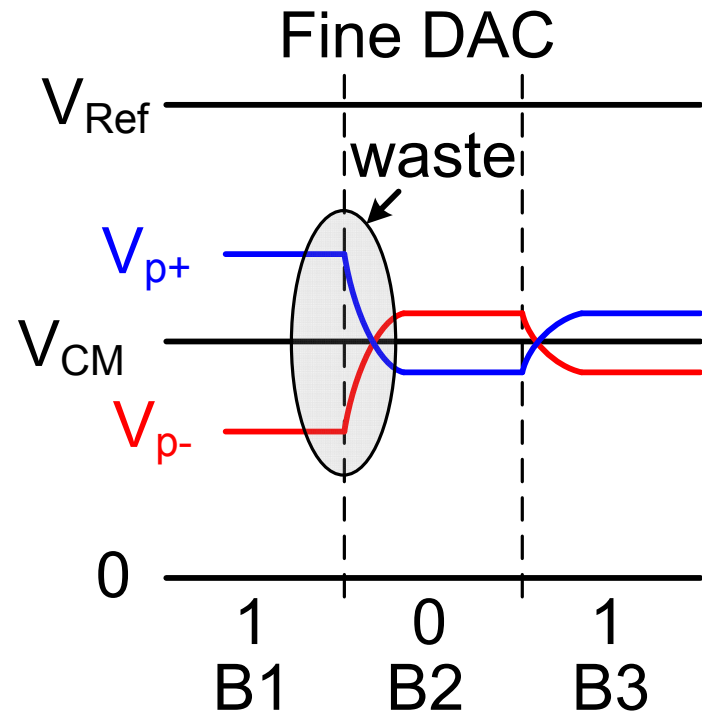
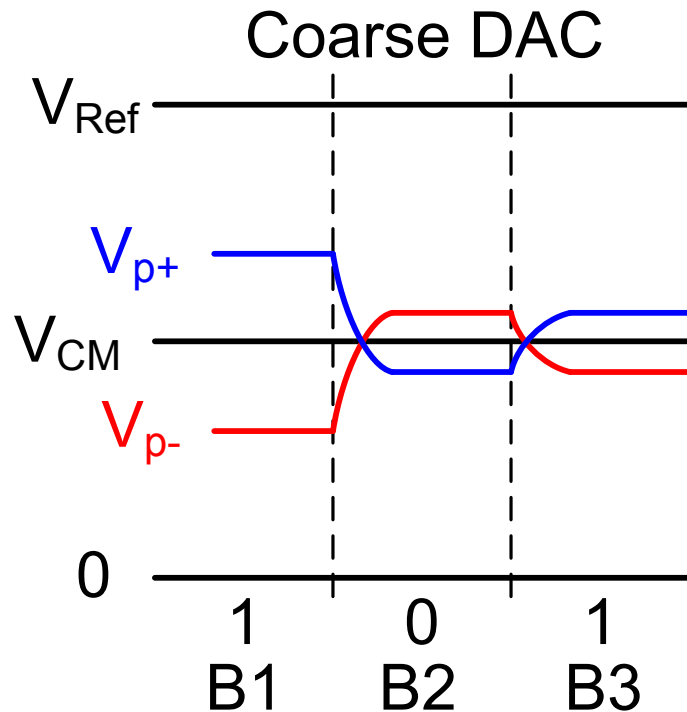
- Small DAC switching energy and settling time
- Low power comparator (C_Cmp)

Fine SAR ADC



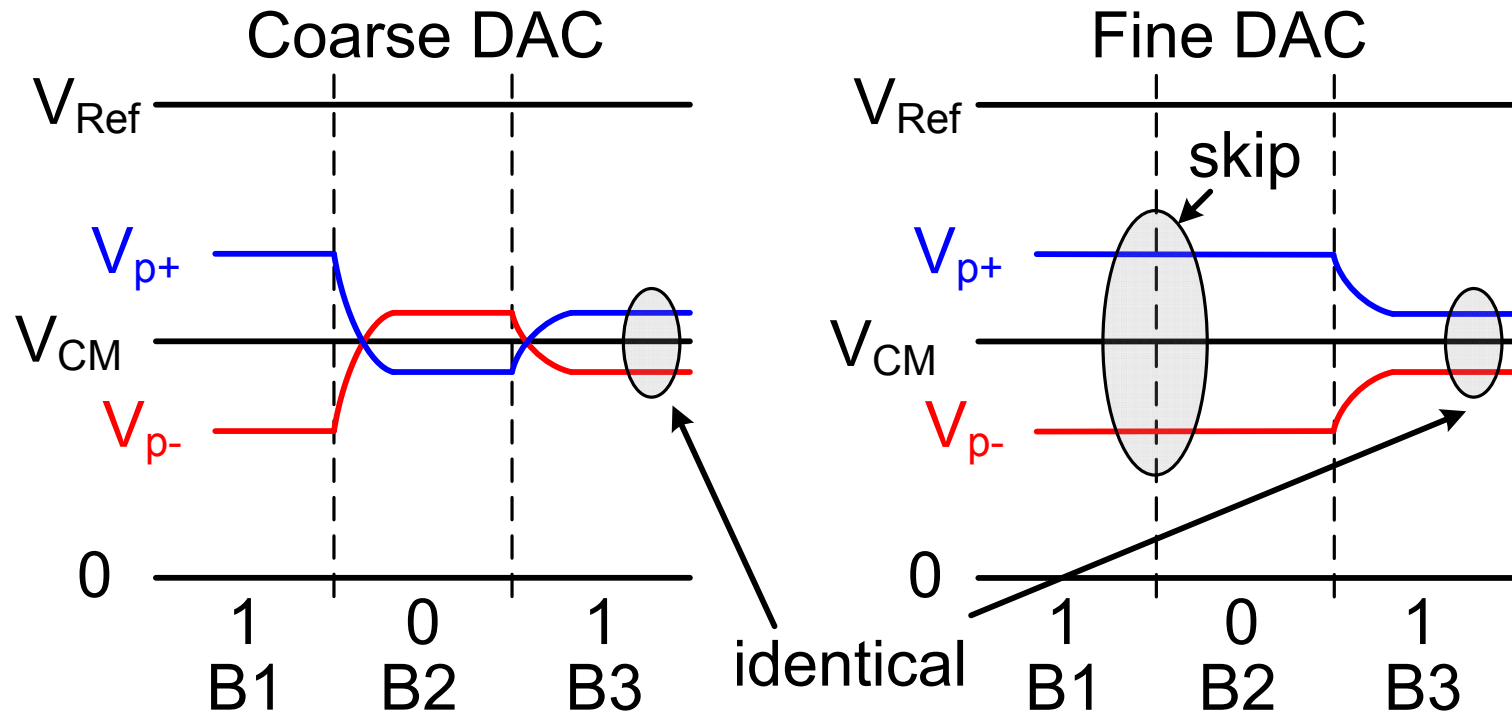
- Only LSB capacitors are switched
- Low noise comparator (F_Cmp)

Switching of MSB Capacitors



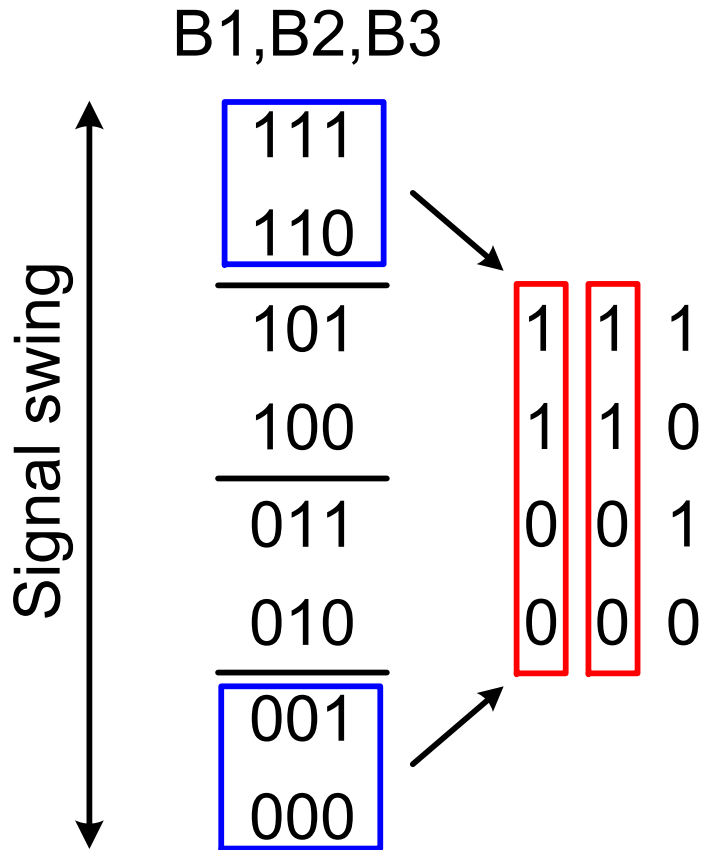
- Fine DAC switching energy is huge
- 3 MSB bits (B1 to B3) as an example

Switching of MSB Capacitors

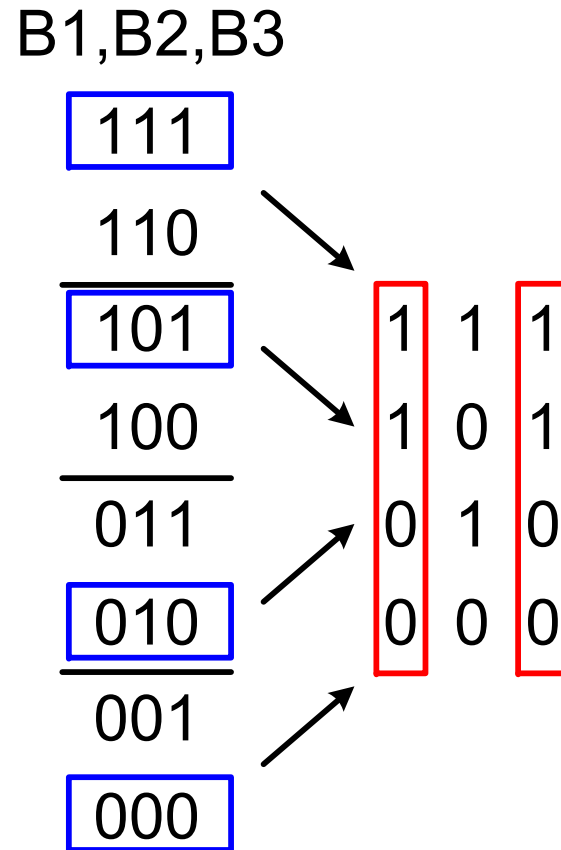


- Avoid MSB capacitors switching of Fine DAC
- Coarse DAC switching energy is negligible

Detect-and-Skip (DAS) Algorithm

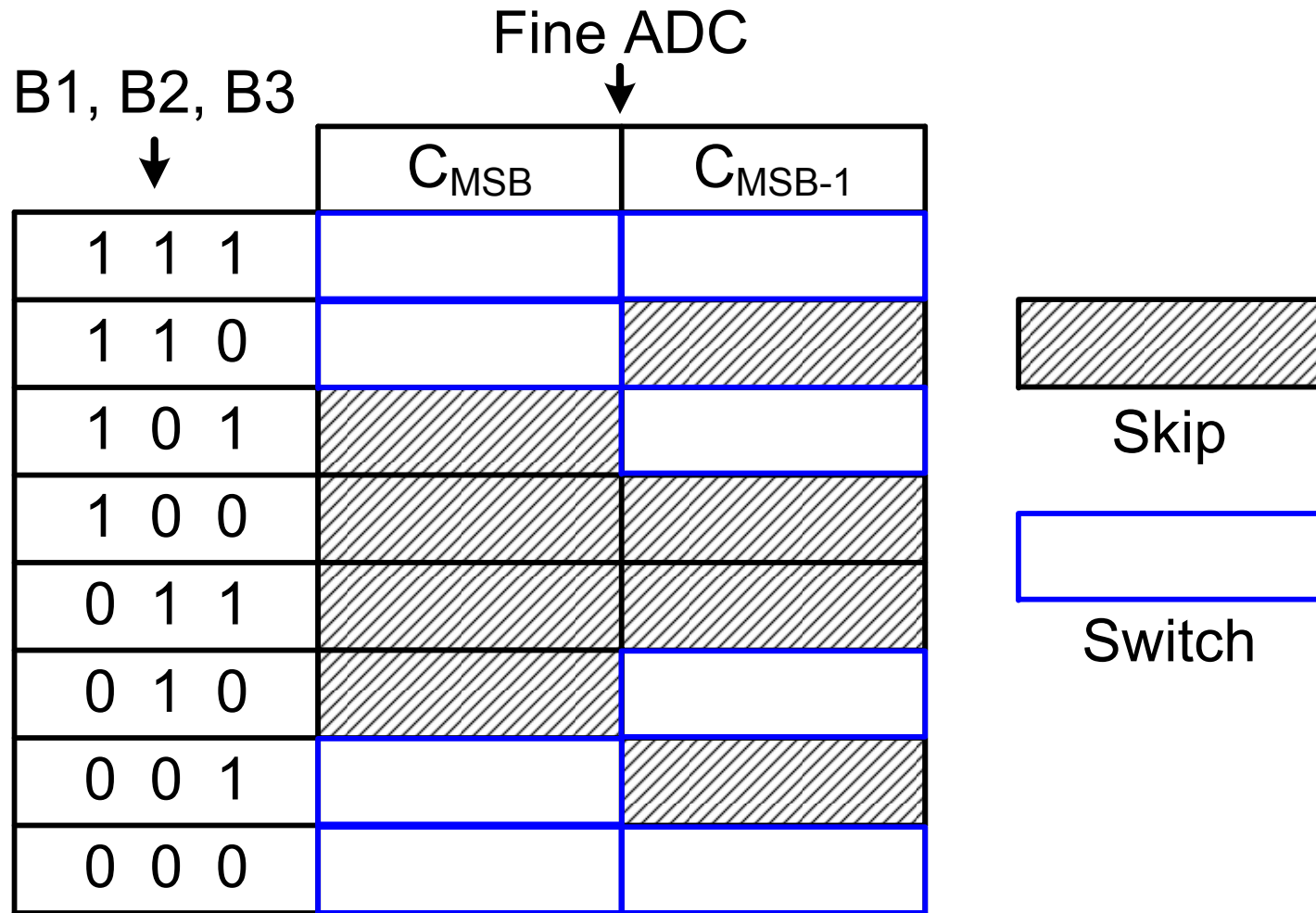


$B1 = B2 \rightarrow \text{Switch } C_{MSB}$



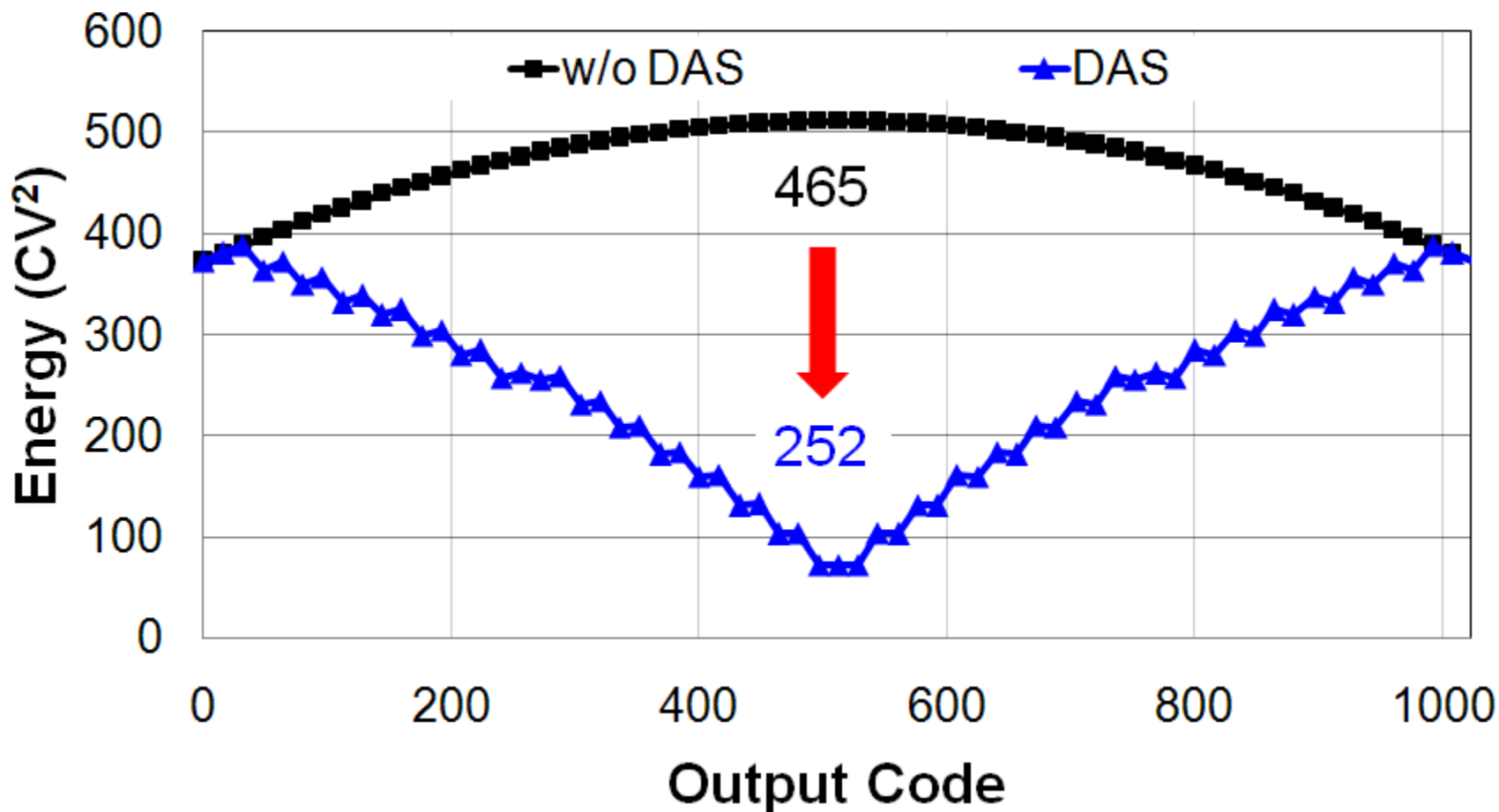
$B1 = B3 \rightarrow \text{Switch } C_{MSB-1}$

Detect-and-Skip (DAS) Algorithm



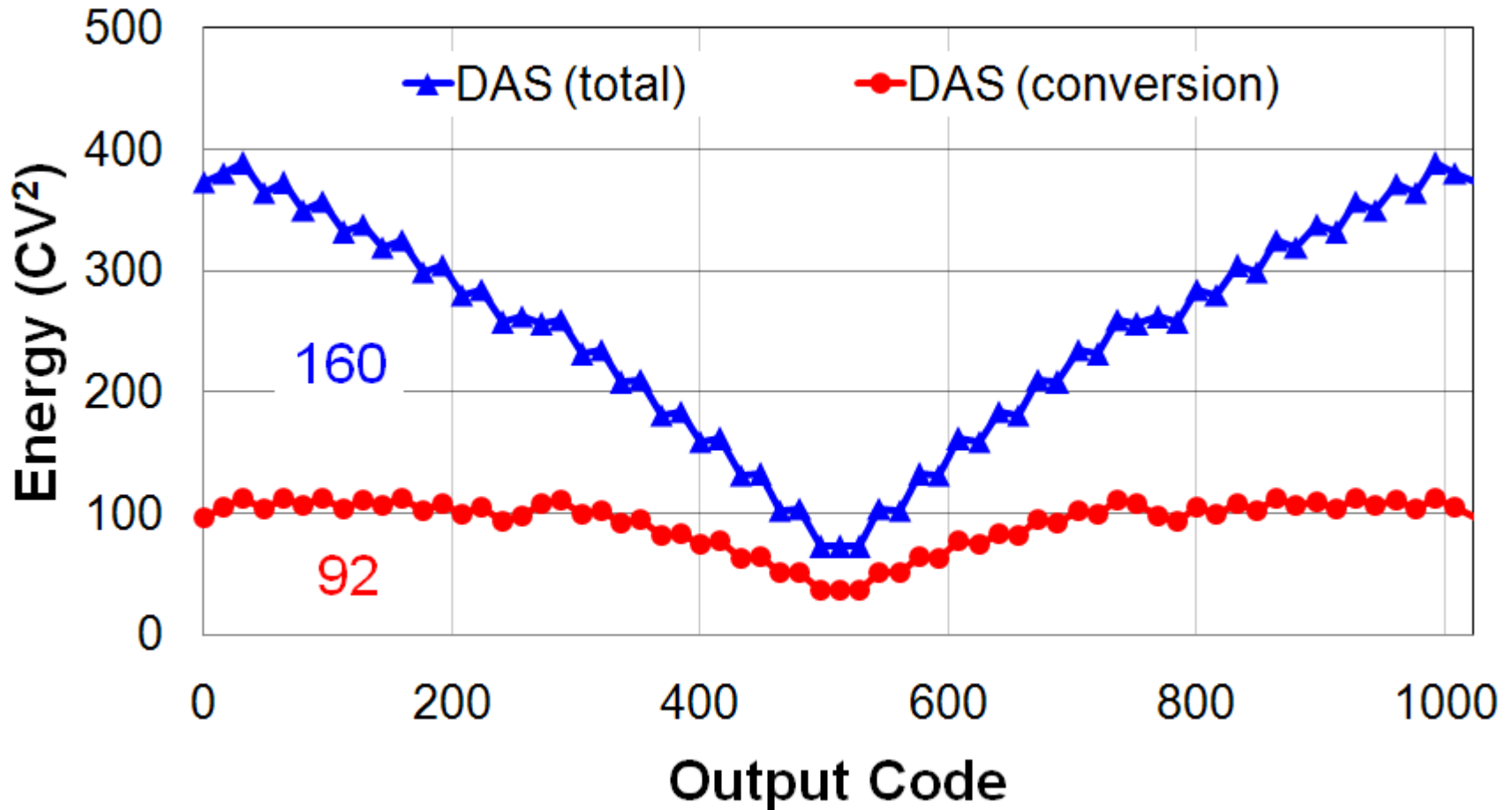
- Save switching energy when input is small

Detect-and-Skip (DAS) Algorithm



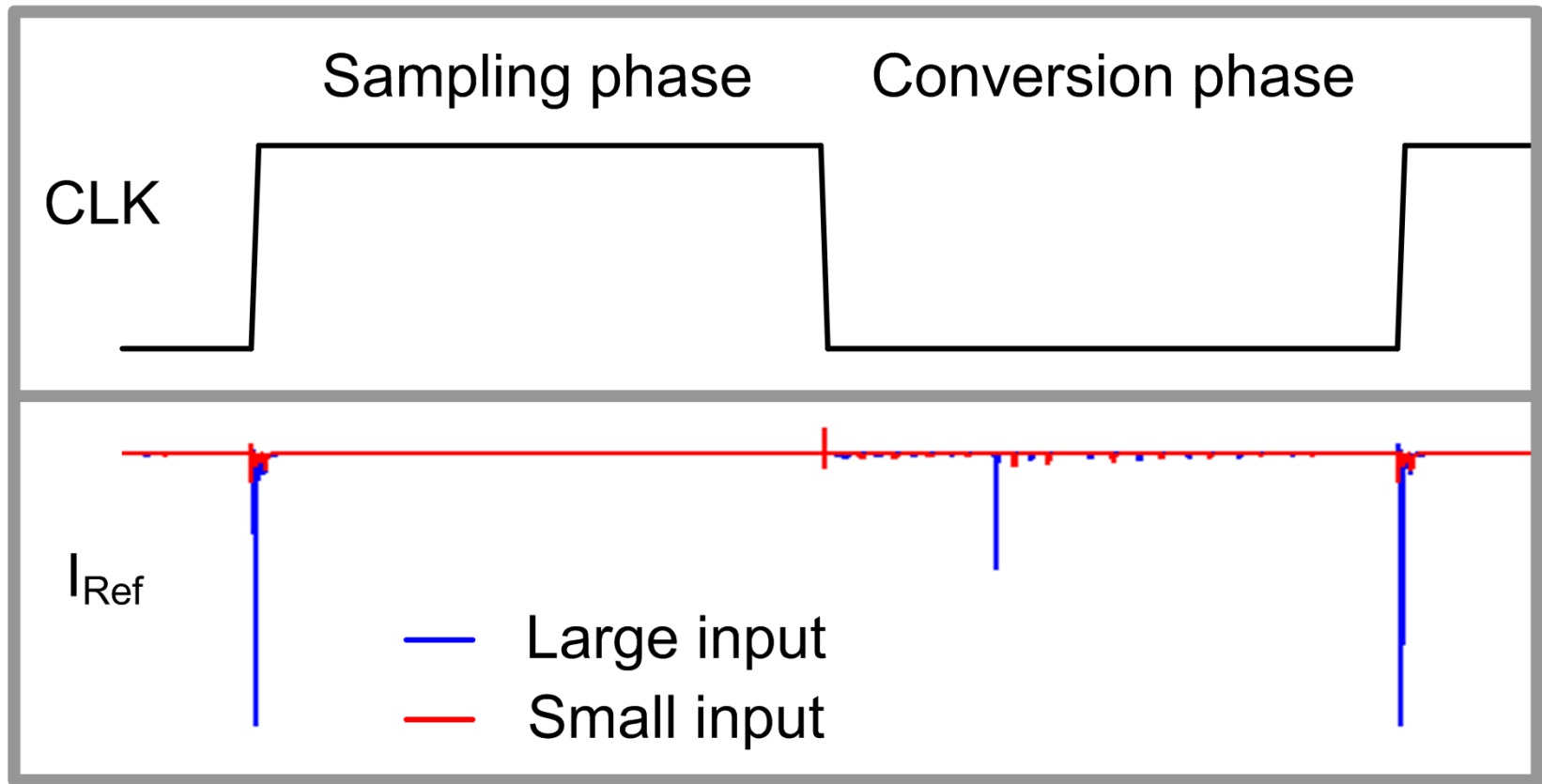
- 5 MSB bits (B1 to B5) use this algorithm

Detect-and-Skip (DAS) Algorithm



- Sampling: 160 CV² & Conversion: 92 CV²

Detect-and-Skip (DAS) Algorithm

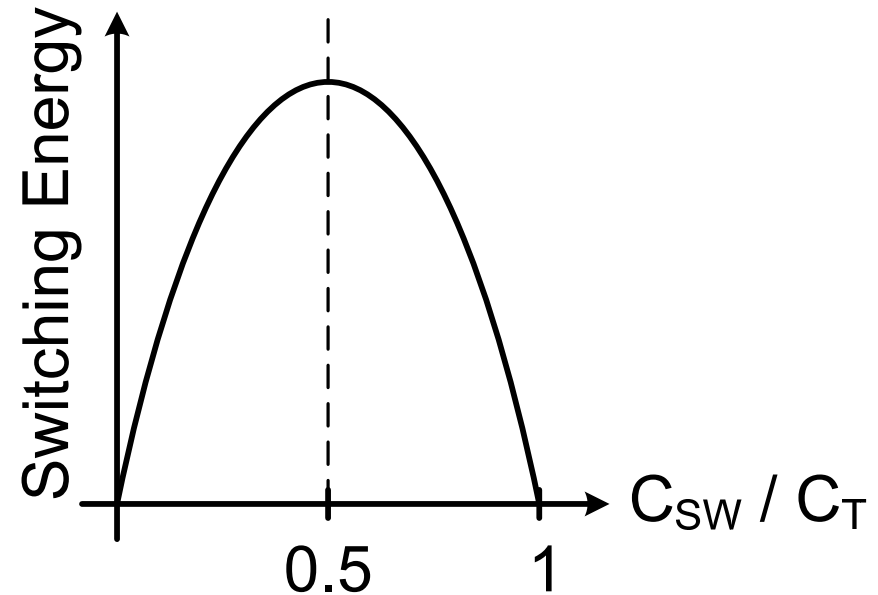
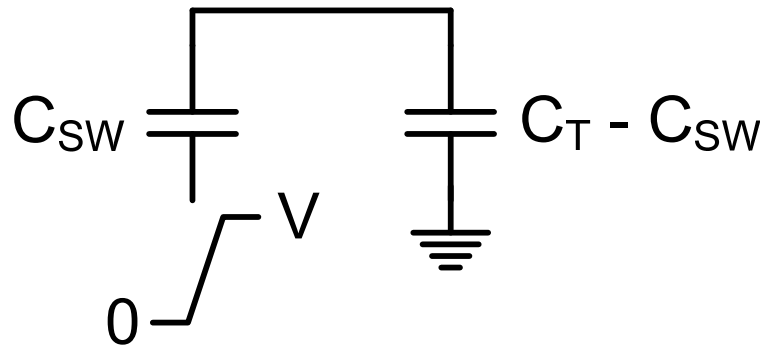


- Low switching energy in conversion phase relaxes reference buffer design

Aligned Switching (AS) Technique

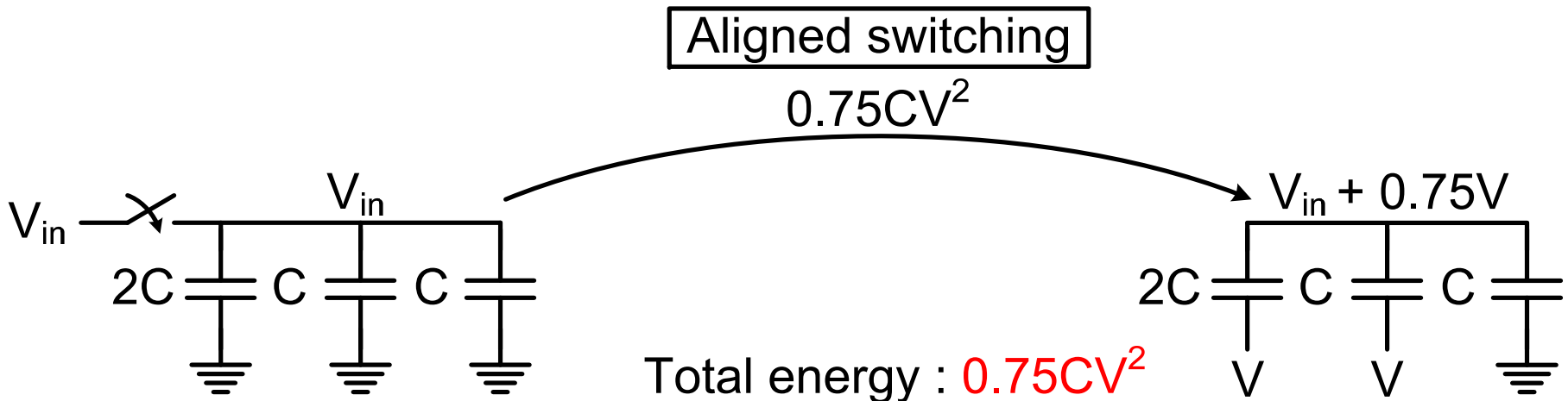
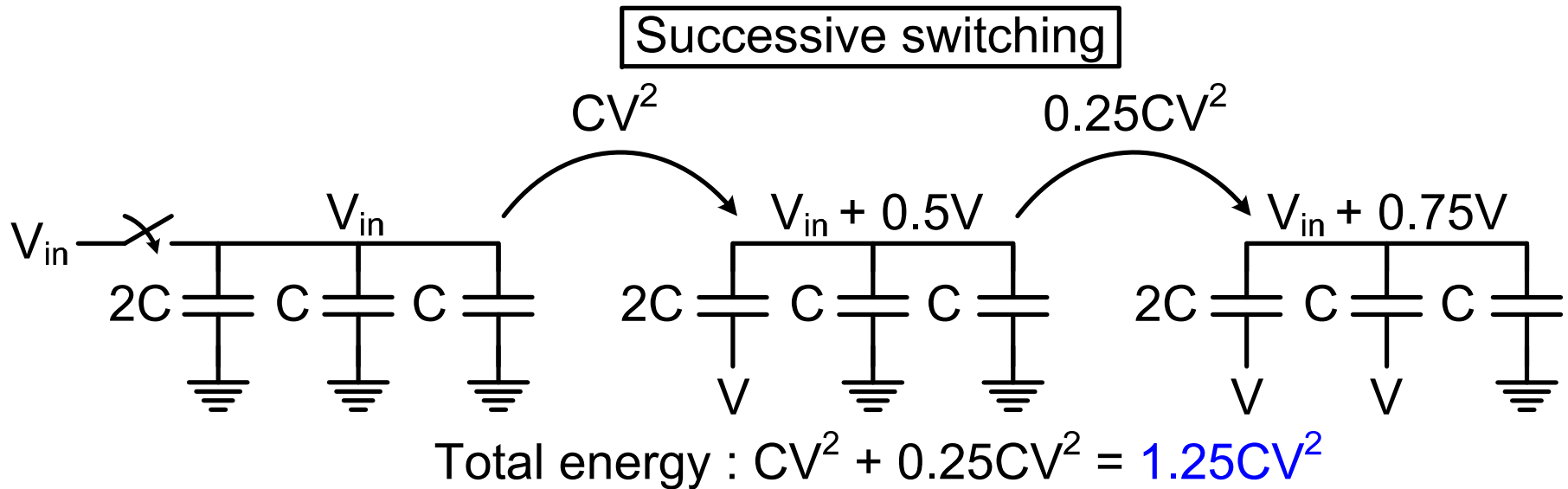
C_T : Total capacitors

C_{SW} : Switched capacitors

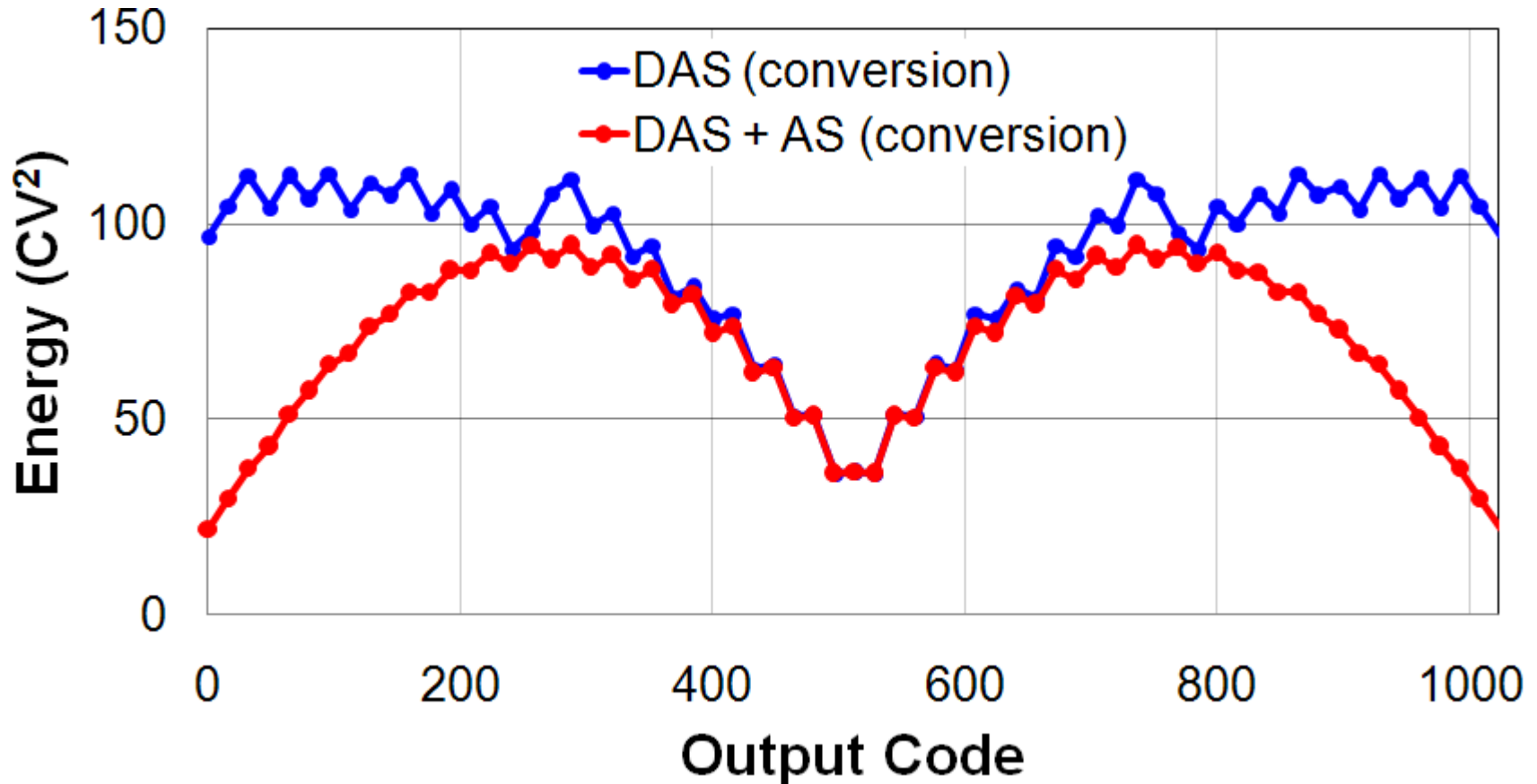


- Switching energy is symmetric to the ratio of 0.5

Aligned Switching (AS) Technique

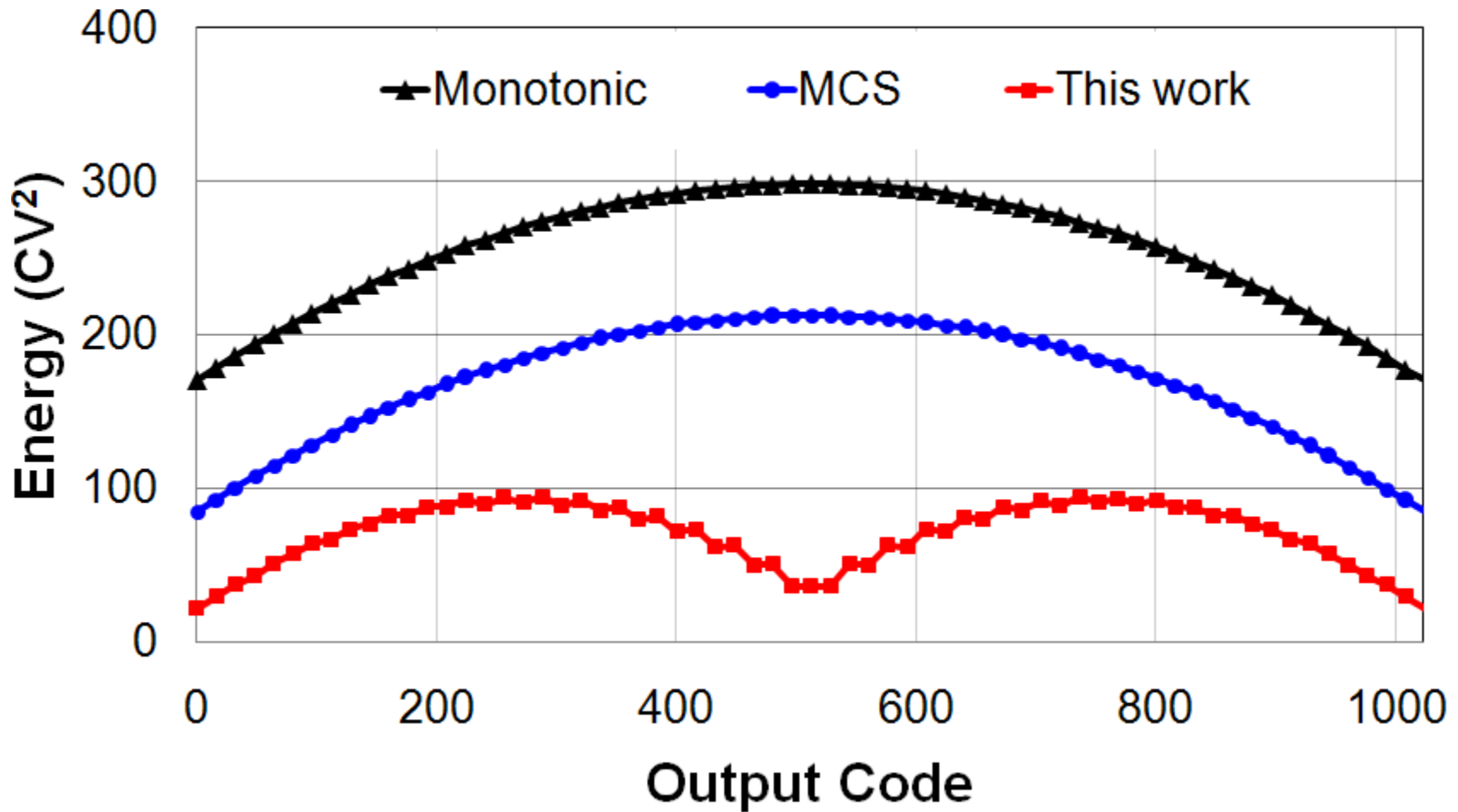


Aligned Switching (AS) Technique



- Conversion: 92 CV² → 70 CV²
- Save switching energy when input is large

DAC Switching Energy Comparison



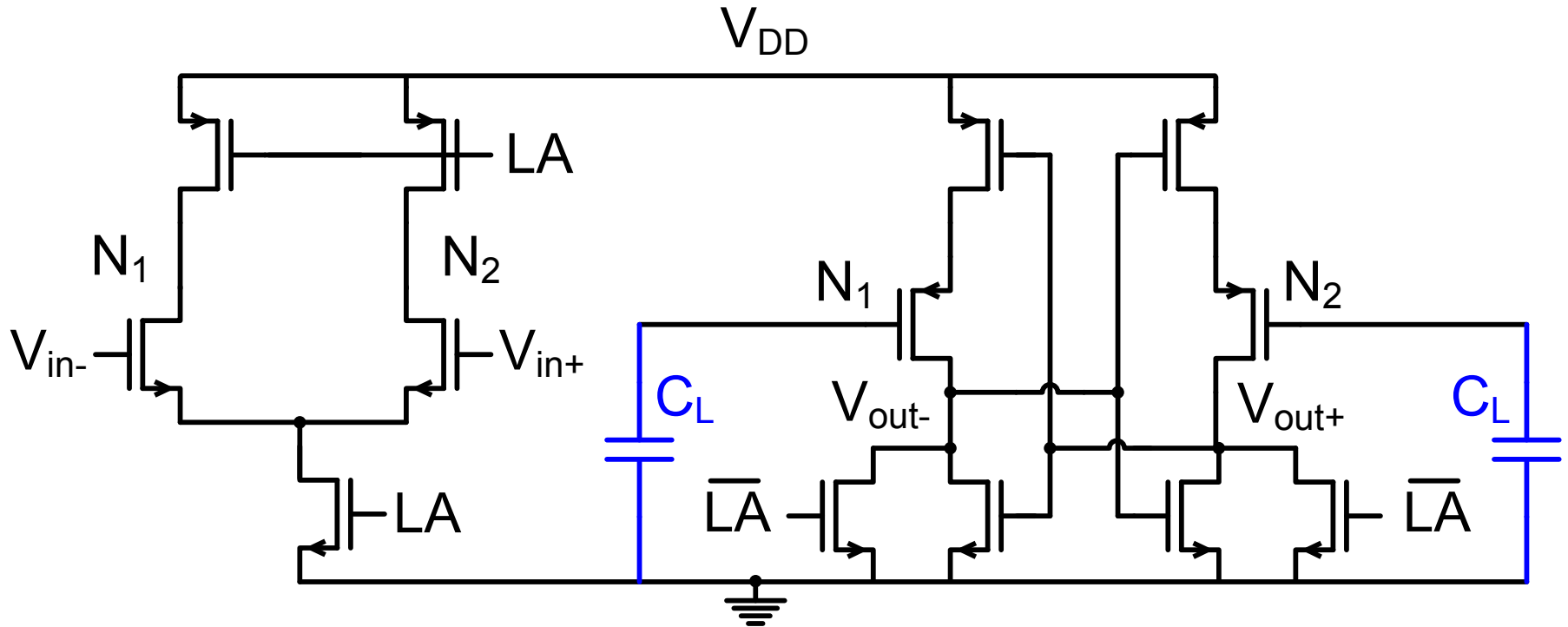
- Switching energy in the conversion phase

DAC Switching Energy Comparison

Switching method	Average energy (CV ²)	
Monotonic	255.5	
MCS	170.2	
This work	229.7	Coarse : 24.7
		Fine : 205
This work (conv. phase)	69.8	Coarse : 9.7
		Fine : 60.1

- Coarse energy << fine energy

Dynamic Comparator



- Power $\propto C_L$
- Noise $\propto 1/\sqrt{C_L}$

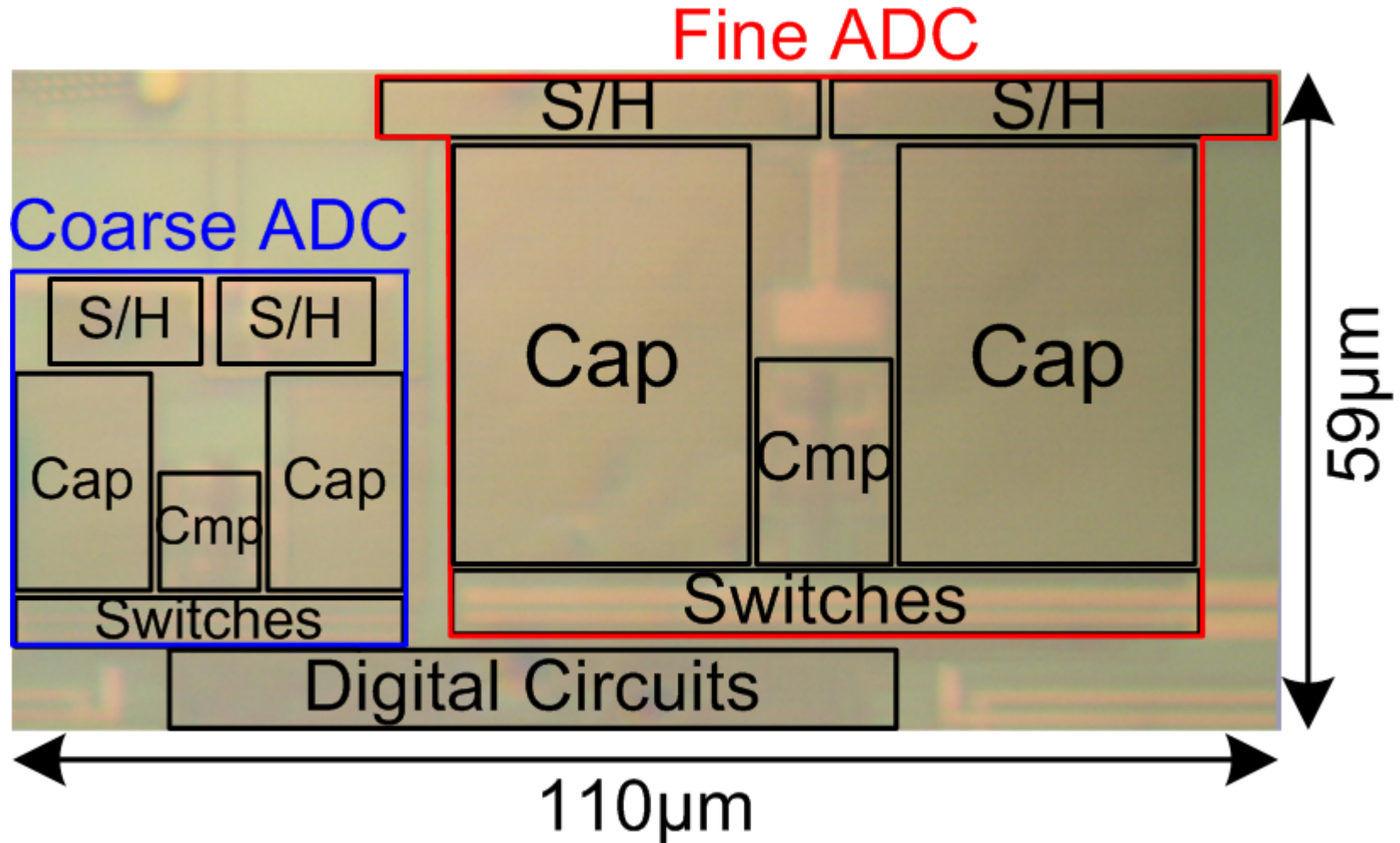
Comparator Noise & Power

	Coarse	Fine
Input-referred noise	0.573 mV _{RMS}	0.391 mV _{RMS}
Power / conversion	1.096 nW	3.287 nW

- Power ratio of fine and coarse comparators is 3
- Conventional 10-bit SAR ADC : $10 \times 3 = 30$
- This work : $1 \times 5 + 3 \times 6 = 23 \rightarrow$ Save 23%

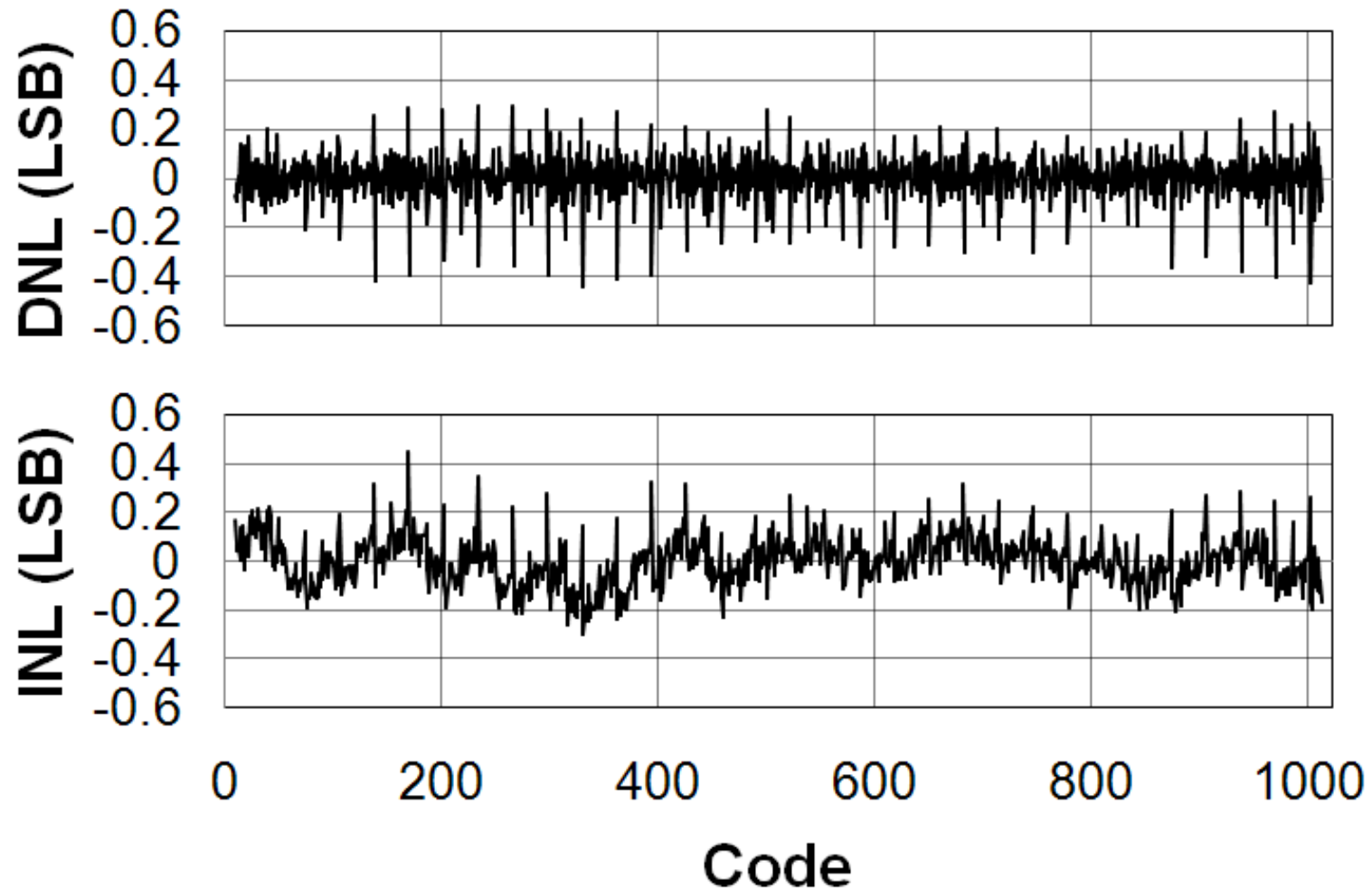
Chip Photo

- 0.0065mm² active area in 40nm CMOS



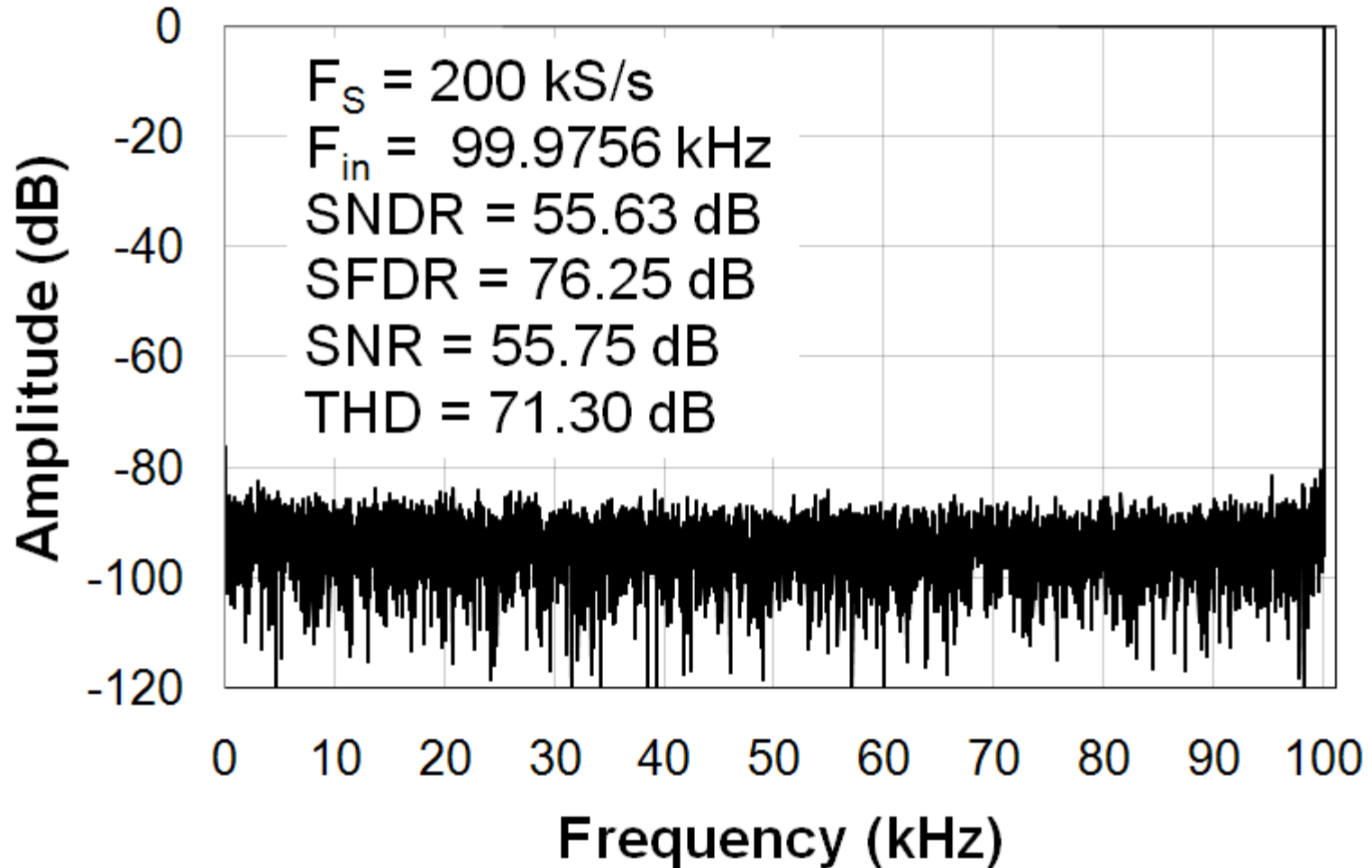
DNL / INL

- DNL = +0.29/-0.44 LSB, INL = +0.45/-0.29 LSB



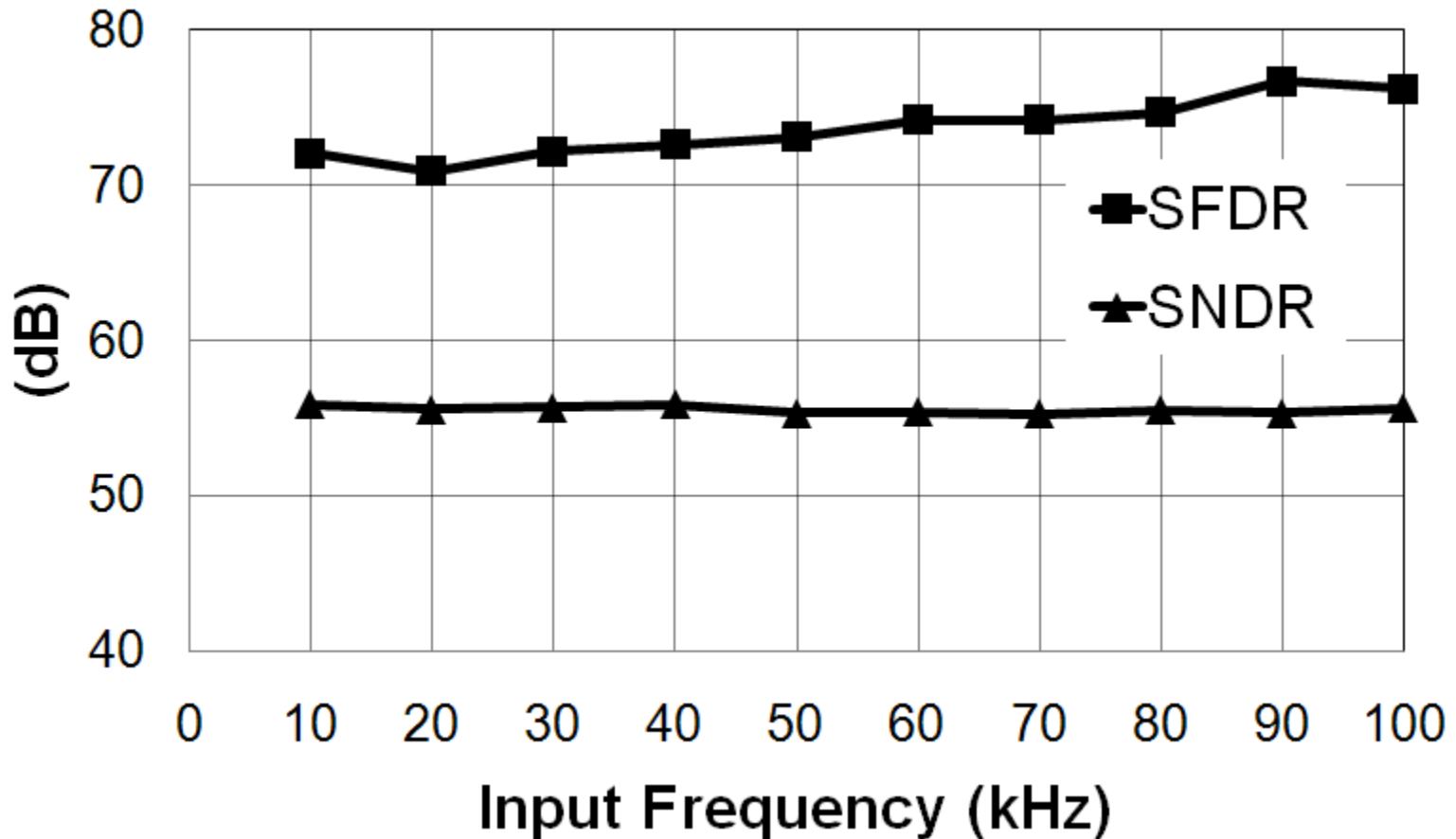
FFT Plot @ Nyquist

- ENOB = 8.95 bits



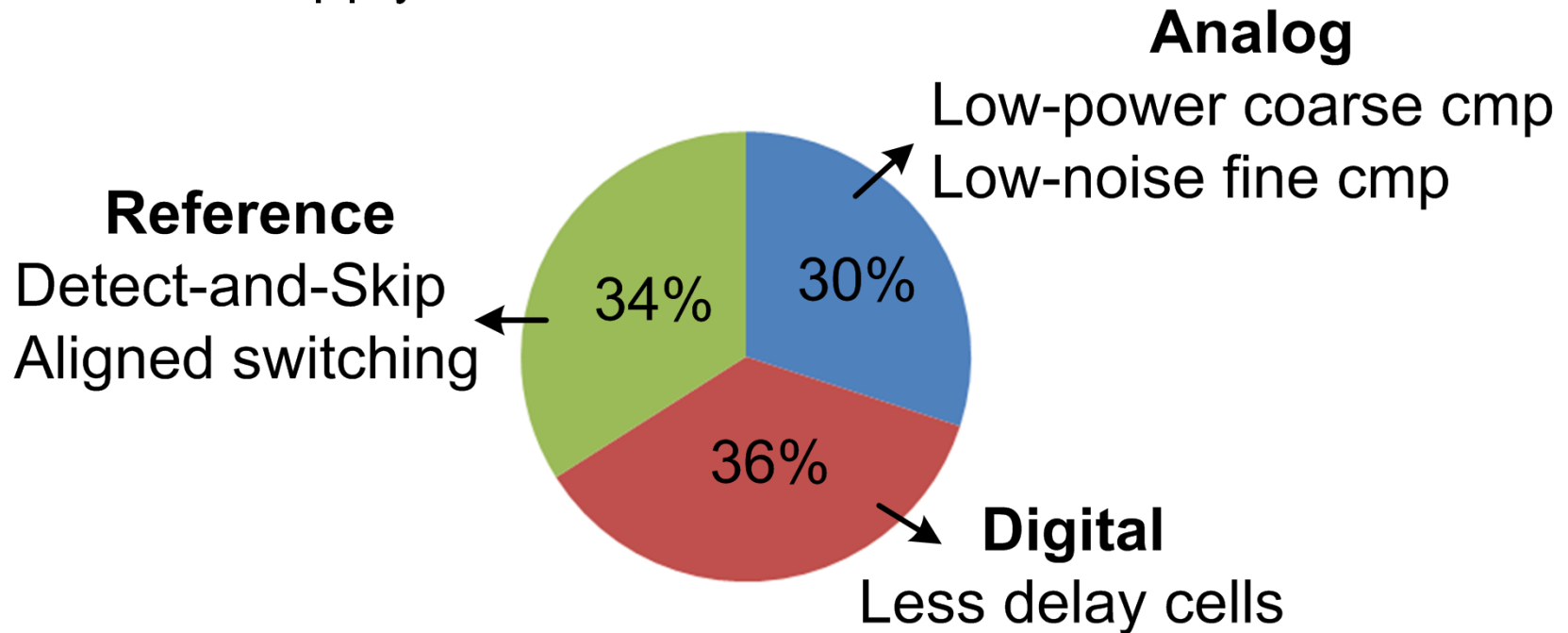
Dynamic Performance

- ENOB ranging from 8.95 to 9 bits



Power Contributions

- **84nW measured at Nyquist input frequency**
 - 40nm CMOS
 - 0.45V supply

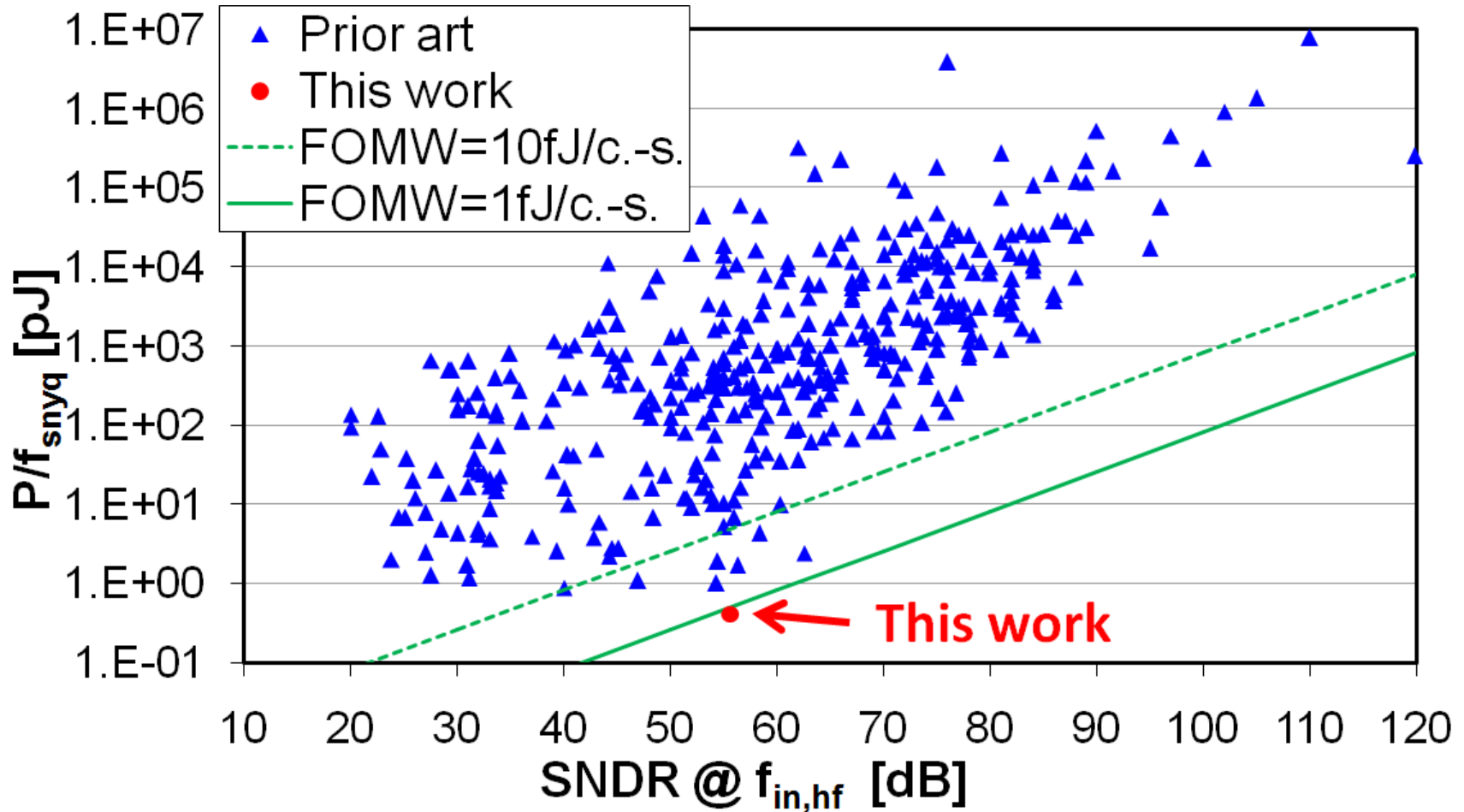


Performance Summary and Comparison

	[1]	[2]	[3]	This work
Technology	90nm	65nm	65nm	40nm
Supply Voltage (V)	0.4	0.6	1	0.45
Sample rate (kS/s)	500	40	1000	200
Power (nW)	500	97	1900	84
ENOB (bit)	8.72	10.1	8.75	8.95
FOMW (fJ/c.-s.)	2.37	2.2	4.4	0.85
Active Area (mm ²)	0.042	0.076	0.026	0.0065

- [1] Liou, ISSCC2013 [2] Harpe, ISSCC2013
[3] Elzaker, ISSCC2008

Performance Comparison



- B. Murmann, "ADC Performance Survey 1997-2013. "
<http://www.stanford.edu/~murmann/adcsurvey.html>.

Conclusion

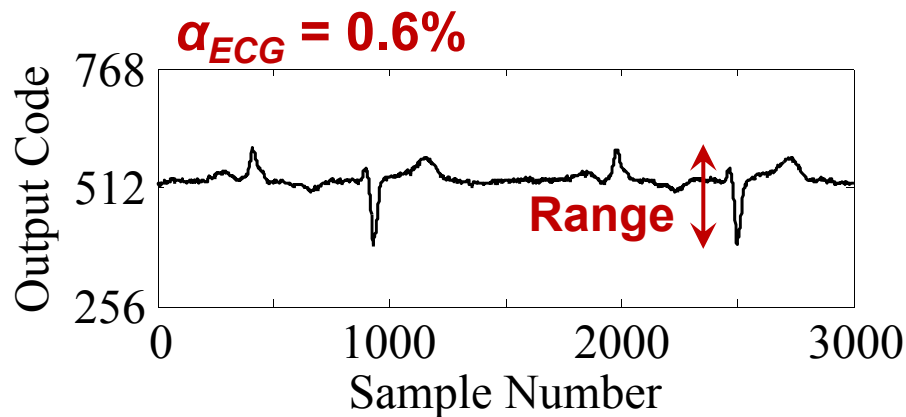
- **Subranging SAR ADC**
 - Coarse ADC reduces power consumption of Fine ADC.
- **DAC power reduction**
 - Detect-and-Skip algorithm for small input
 - Aligned switching technique for large input
- **Comparator power reduction**
 - 23% saving by 1-bit redundancy
- **Overall performance**
 - FOMW is lower than 1 fJ/conversion-step.

A 10b 0.6nW SAR ADC with Data-Dependent Energy Savings Using LSB-first Successive Approximation

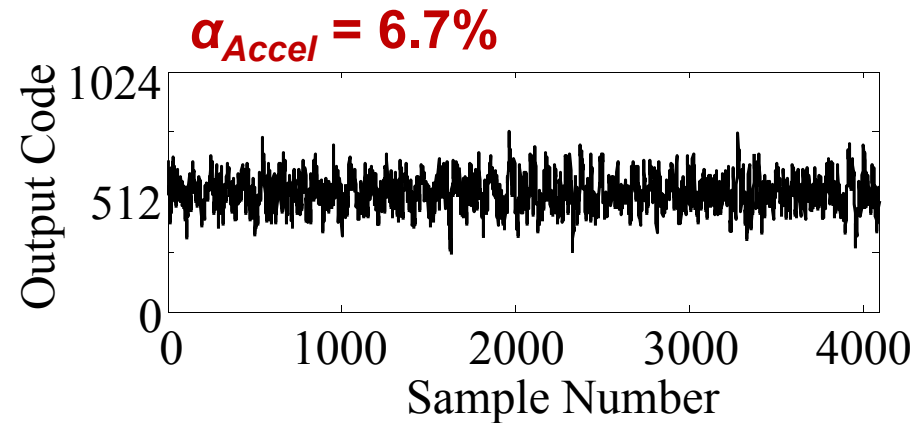
Frank M. Yaul and Anantha P. Chandrakasan
Massachusetts Institute of Technology

Low-Activity Signals

- On average, what fraction of its full range does the signal jump from sample to sample?
- Signal activity: $\alpha = \frac{\langle \Delta code \rangle}{Range}$



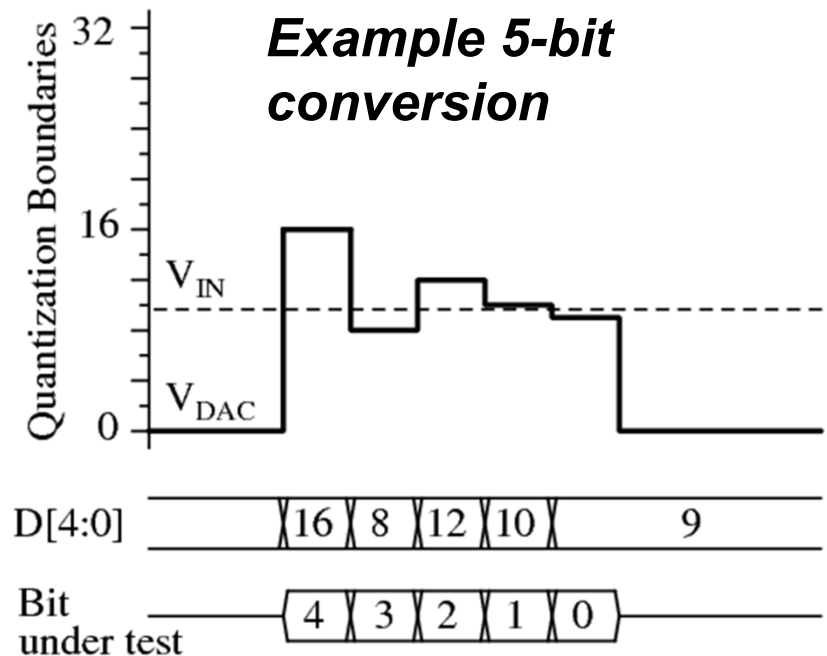
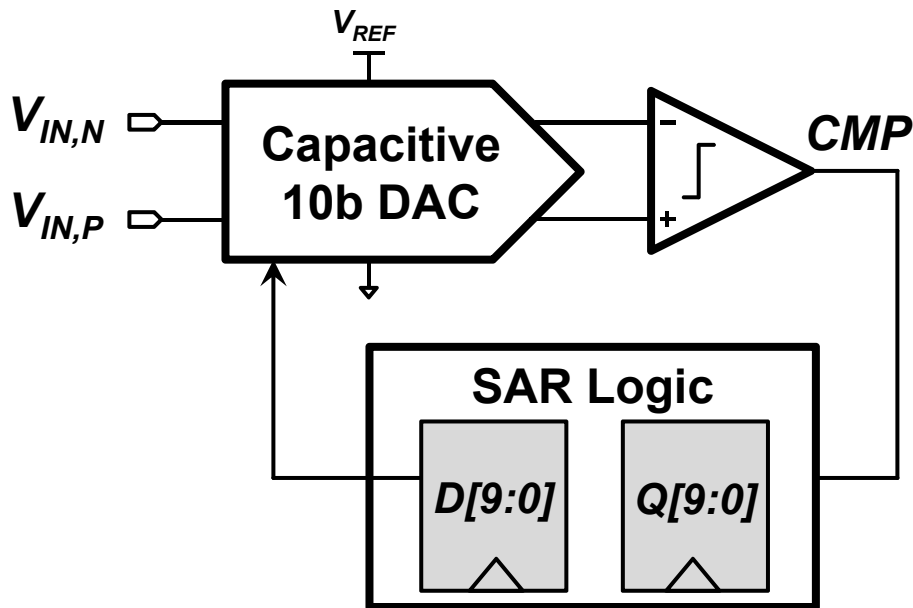
ECG Signal, 1 kS/s



Vibration Signal, 5 kS/s

A/D Conversion with Conventional SA

- SAR ADCs show best FOM in the 8-12b 0-1MS/s range



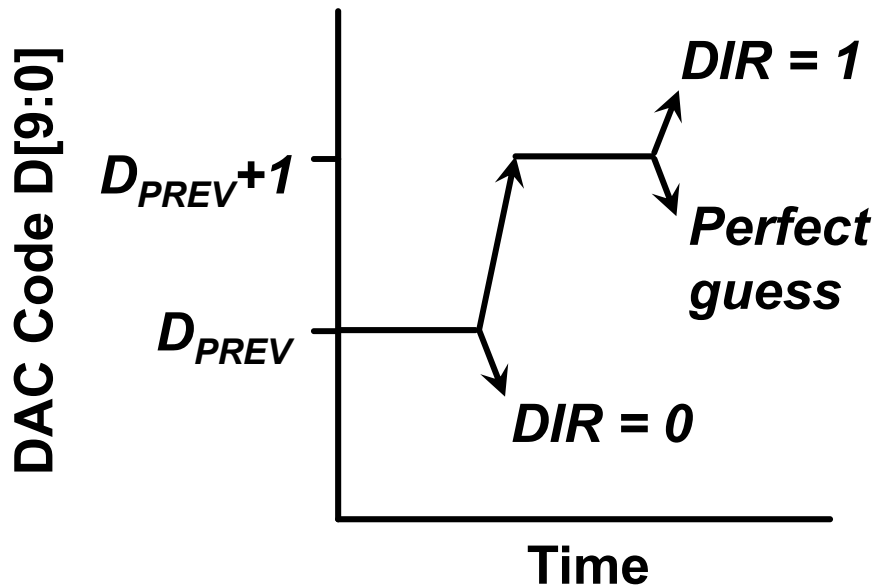
- Conventional SA always uses same initial guess
- Can we alter the algorithm to exploit low signal activity?***

LSB-first SA Overview

Key Idea: Start search with initial guess (previous sample D_{PREV}). Use fewer bitcycles when initial guess is close to final output code D_{OUT} .

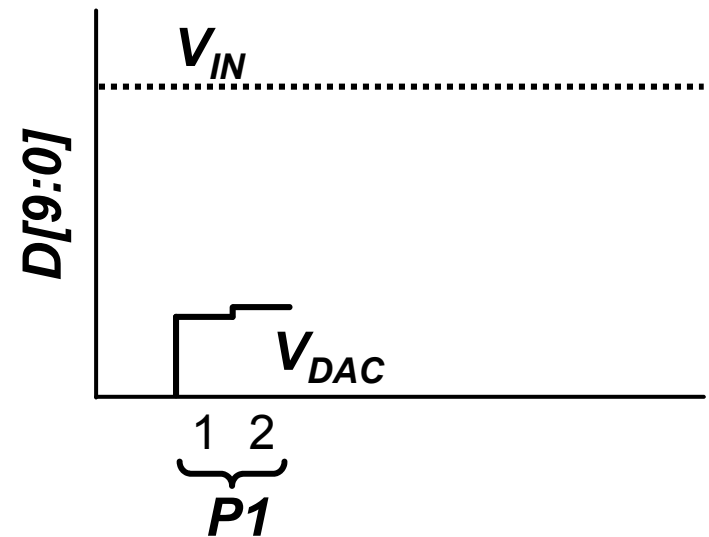
P1: INIT Phase

Determine DIR , the error direction of the initial guess



Example 10b conversion:

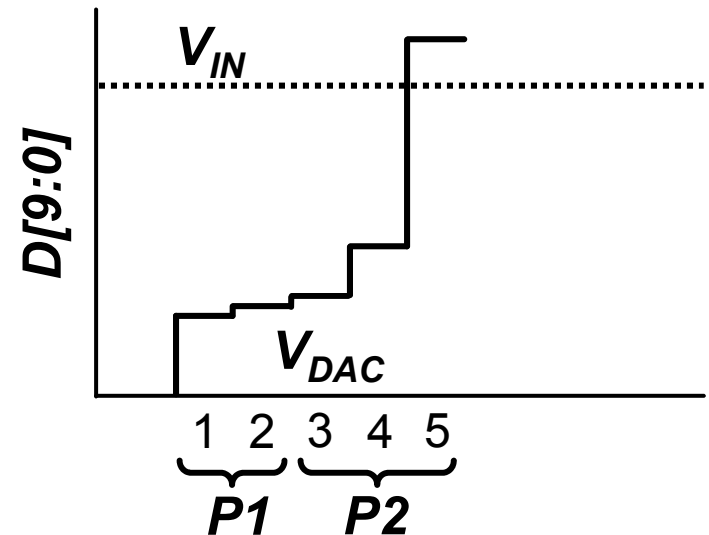
$$D_{PREV} = 842, D_{OUT} = 860$$



P2: To MSB Phase

- Set bits in D to D/IR from LSB to MSB until V_{DAC} overshoots V_{IN} . Skip bits already set correctly.

Bitcycle	$D[9:0]$	CMP
1,2	11010 01010	Lo
3	11010 0101 1	Lo
4	11010 01 1 11	Lo
5	11010 1 1111	Hi

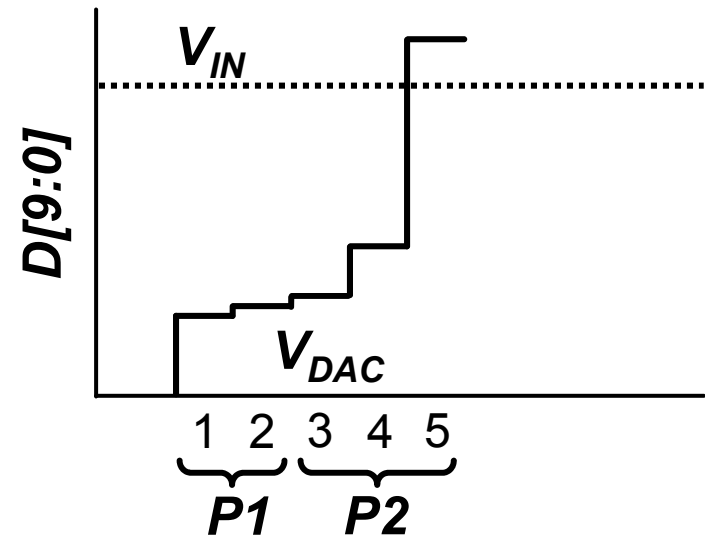


P2: To MSB Phase

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Bitcycle	$D[9:0]$	CMP
1,2	11010 01010	Lo
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5	11010 1 1111	Hi

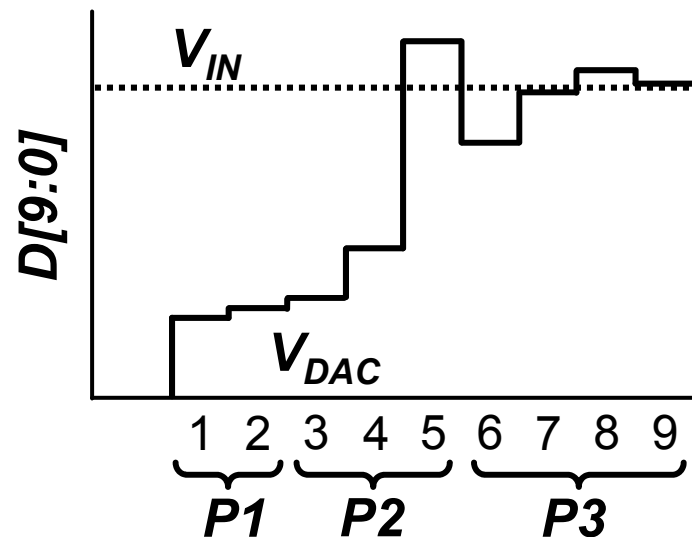
$D_{OUT} = 11010 \ 1XXXX$



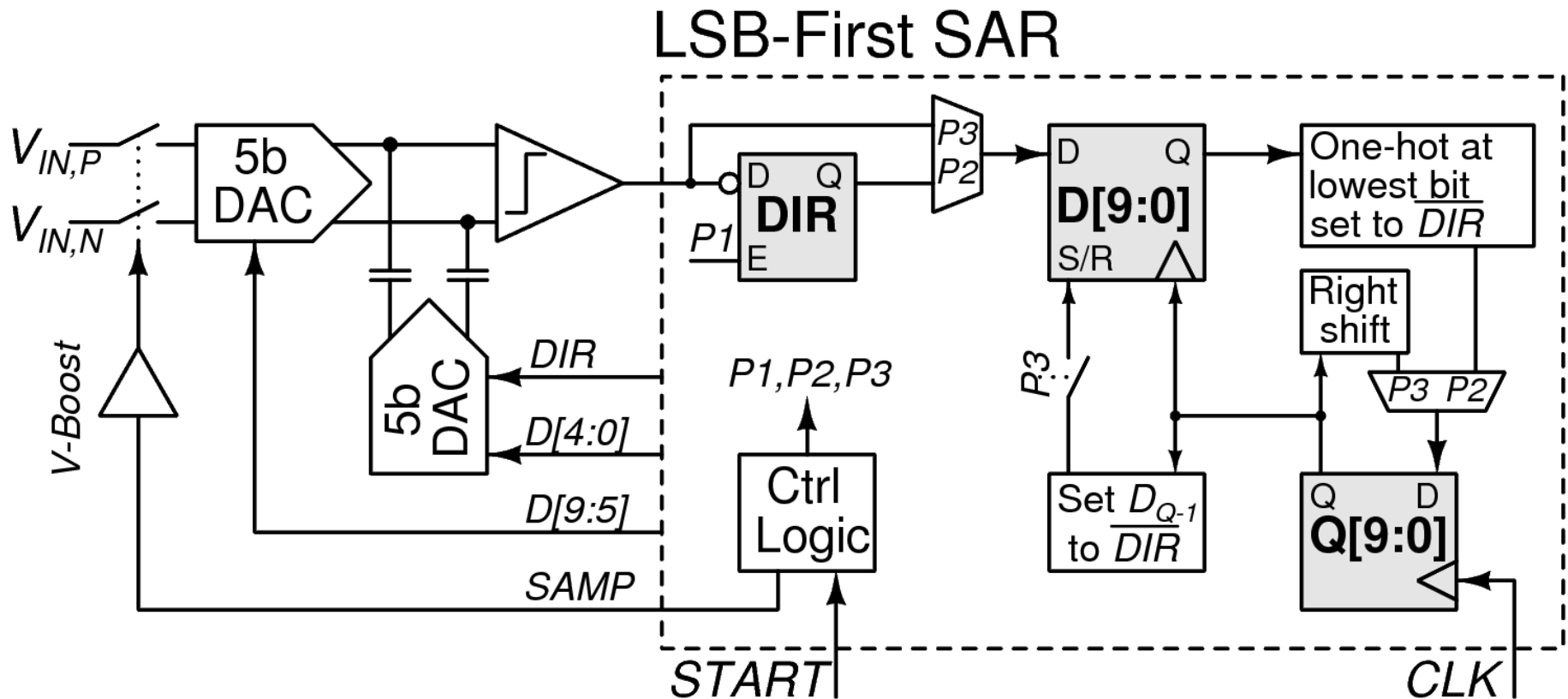
P3: To LSB Phase

- Perform conventional SA back towards LSB
- Must account for *DIR*

Bitcycle	$D[9:0]$
5	11010 11111
6	11010 1 0 111
7	11010 11 0 11
8	11010 111 0 1
9	11010 1110 0

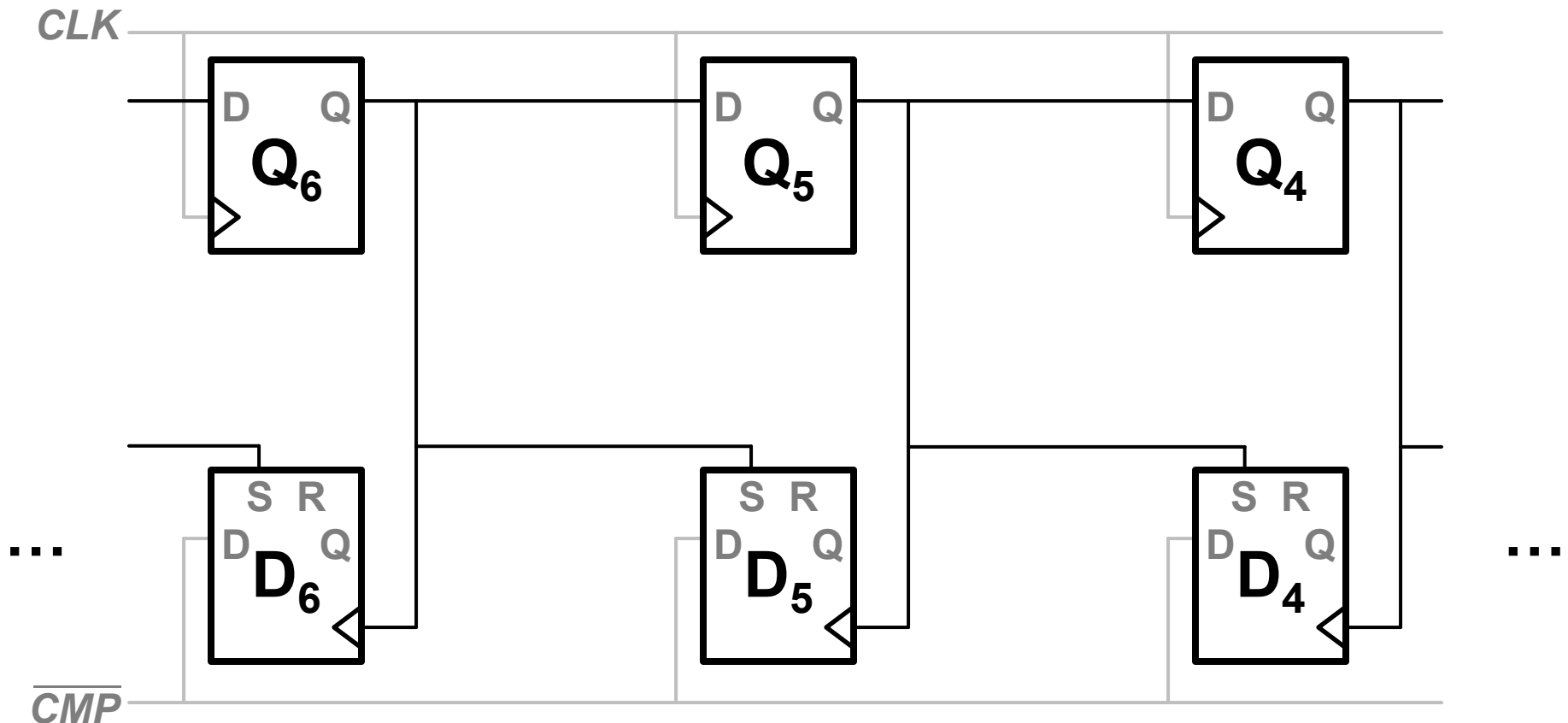


- 2 registers per bit
- Extra combinational logic implements LSB-first SA



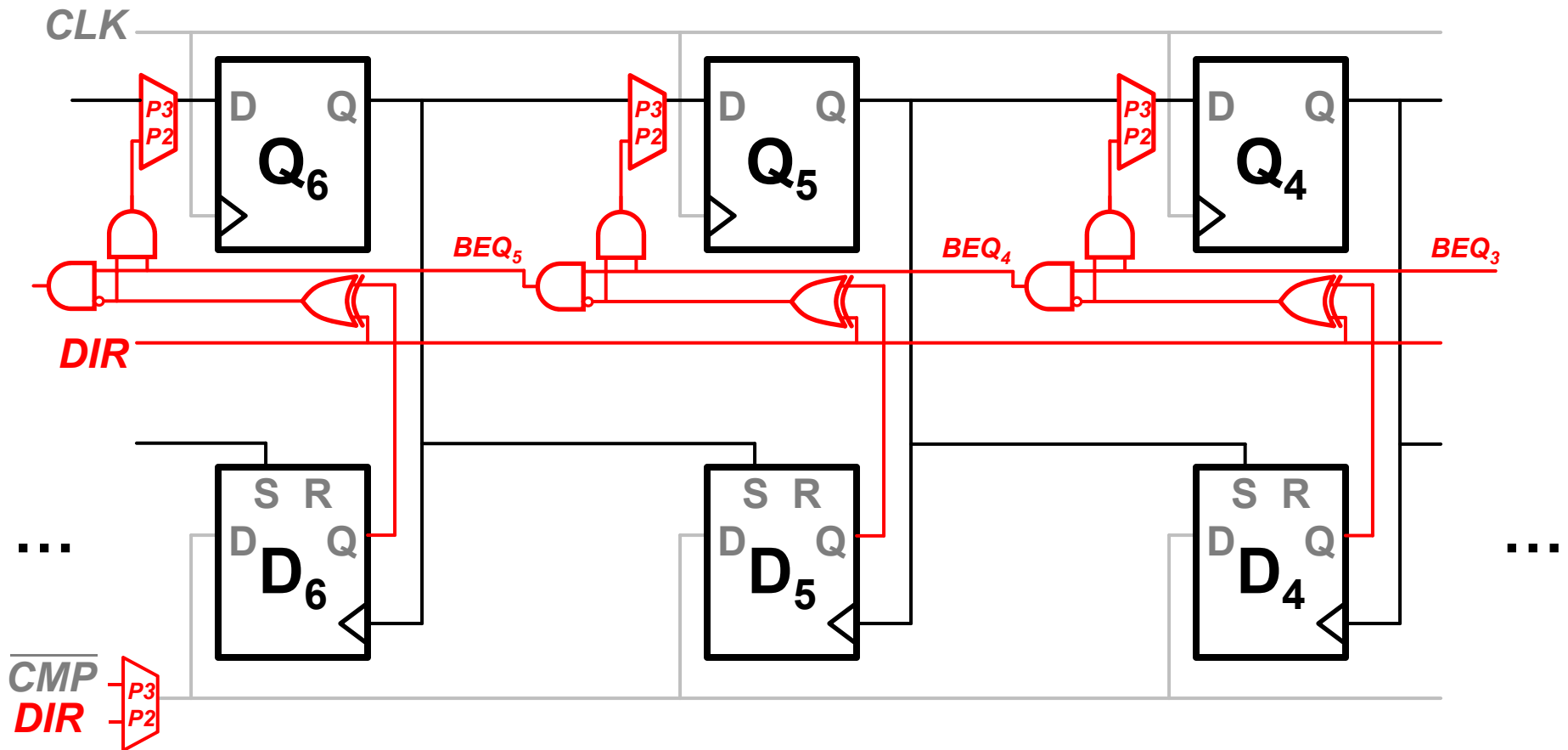
LSB-first SAR Logic

- **P2:** ToMSB Phase
- **P3:** ToLSB Phase



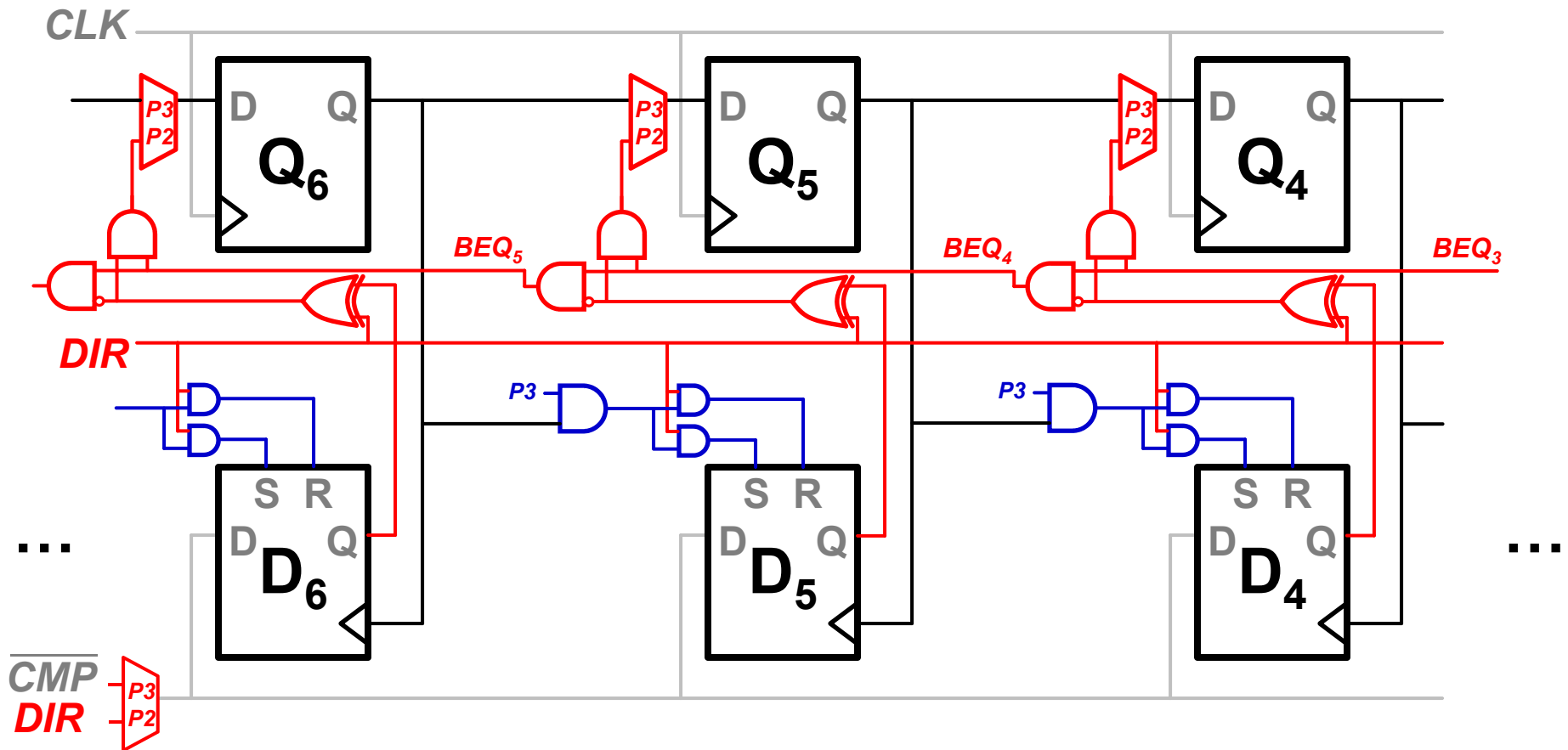
LSB-first SAR Logic

- **P2:** ToMSB Phase
- **P3:** ToLSB Phase



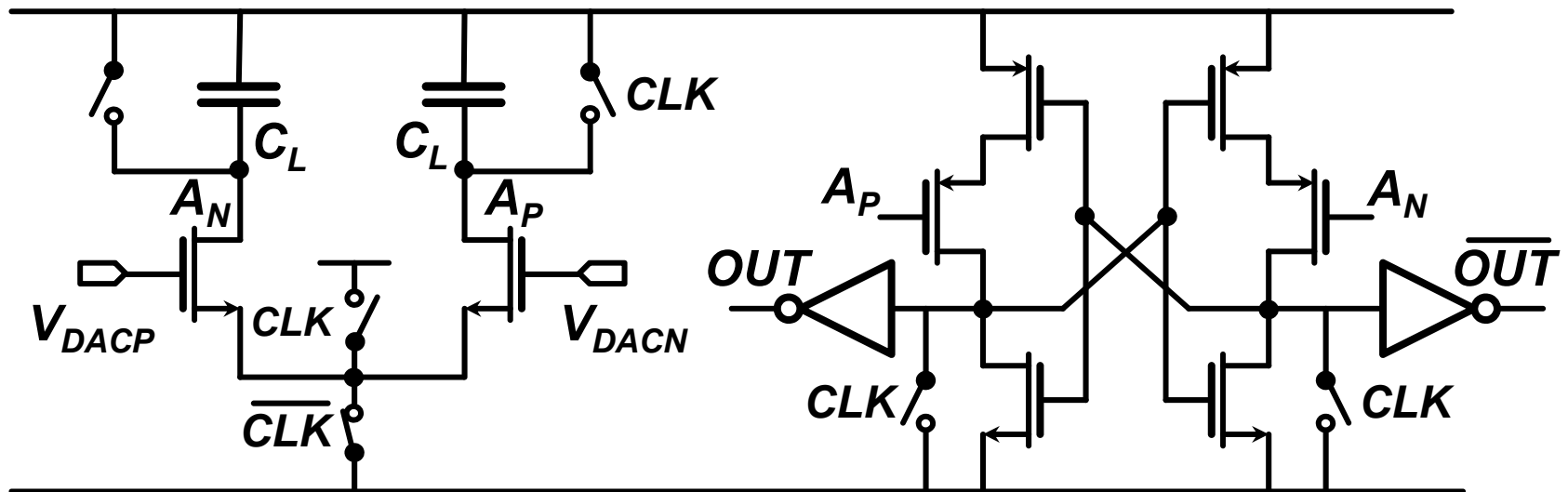
LSB-first SAR Logic

- **P2:** ToMSB Phase
- **P3:** ToLSB Phase



Dynamic Comparator

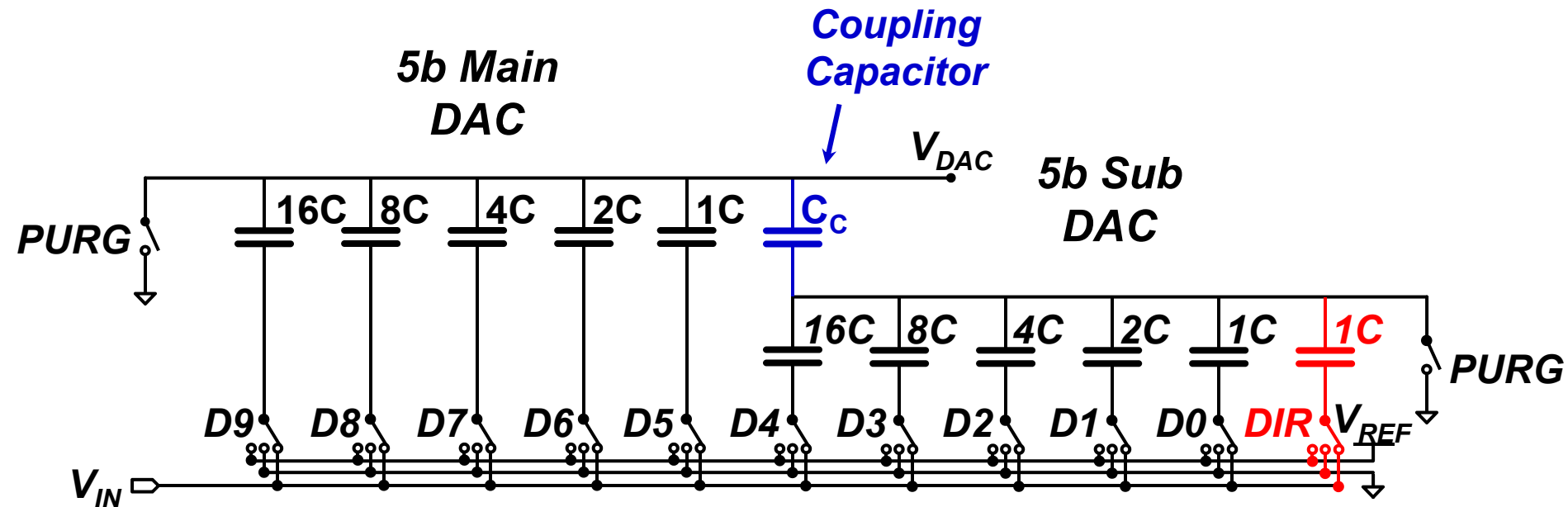
- Gain stage and latch
- Low- V_T input pair improves speed at low V_{DD}



[M. Van Elzakker et al., *ISSCC 2008*]

10b Capacitive DAC

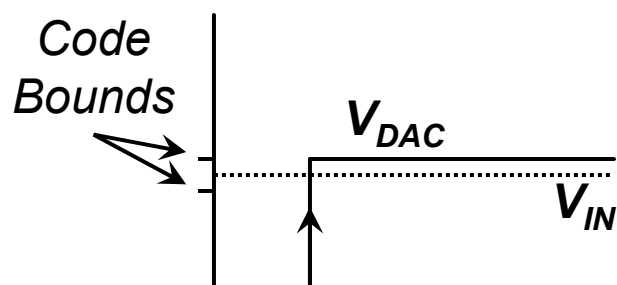
- Uses 2^6 unit capacitors rather than 2^{10}
- Bottom-plate sampling



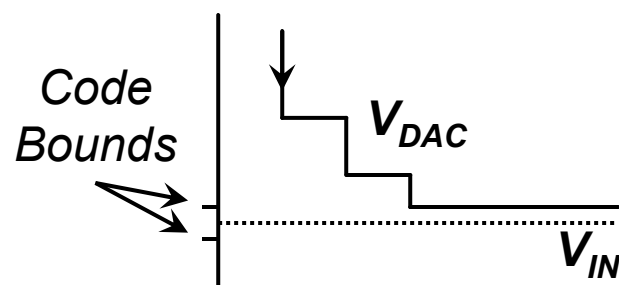
Extra LSB capacitor allows generation of either upper or lower code boundary for a given input code

Code Boundary Issues

- For ***DIR = 1***, set V_{DAC} to test code ***upper*** bound



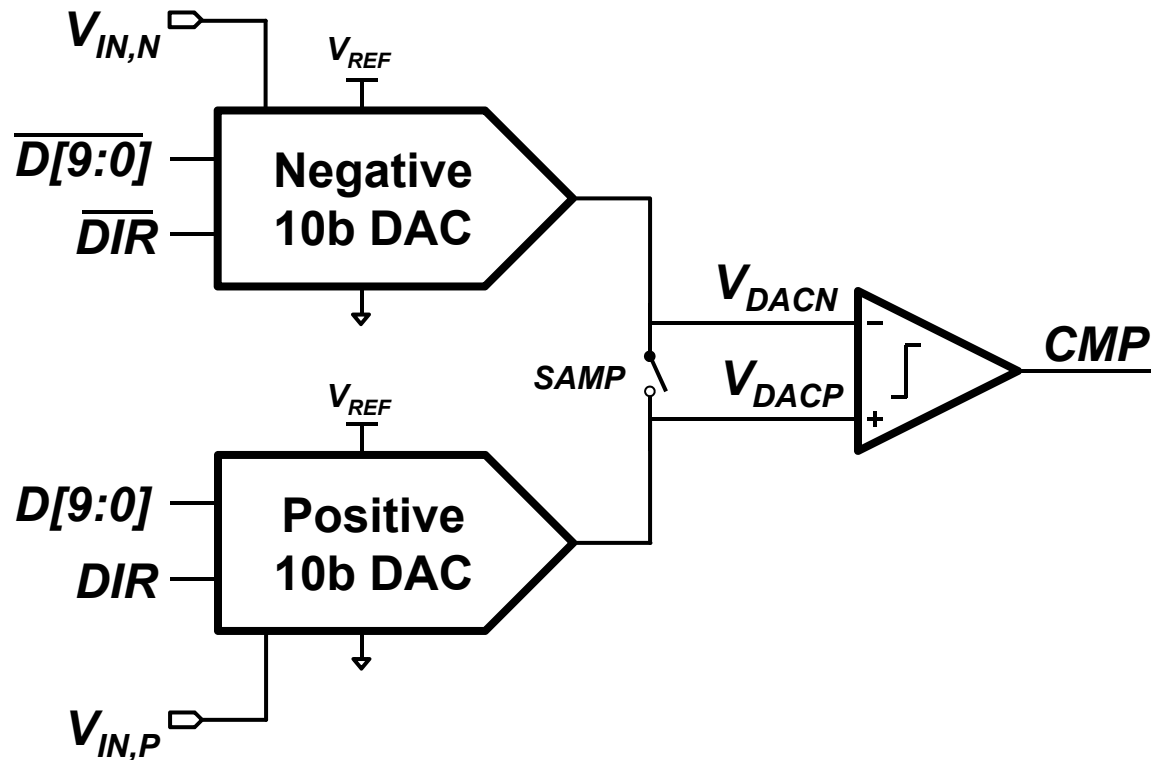
ToMSB: Check ***upper*** code bound when checking for ***positive*** overshoot.



ToLSB: Check ***upper*** code bound when using a test value of ***0***

- For ***DIR = 0***, set V_{DAC} to test code ***lower*** bound

10b Capacitive DAC

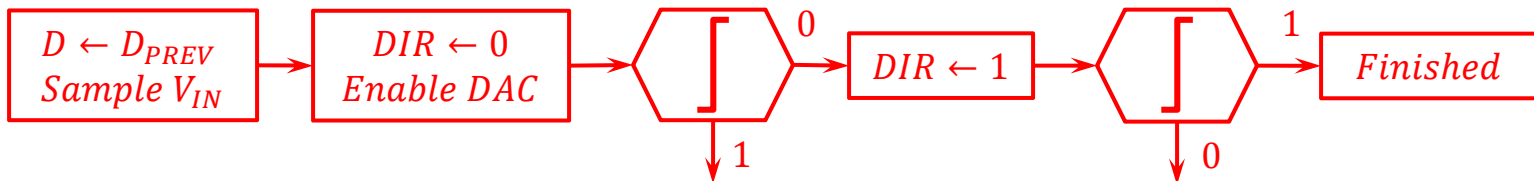
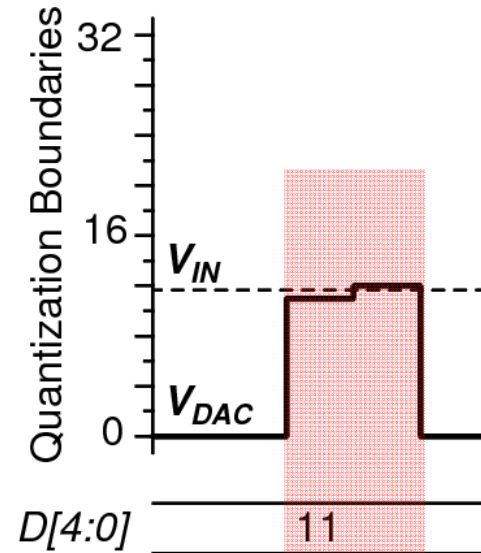


Differential architecture

LSB-first SA: Best Case

$$D_{PREV} = 11, D_{OUT} = 11$$

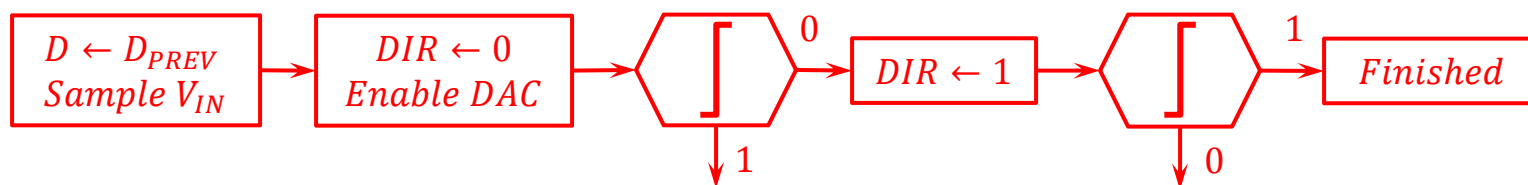
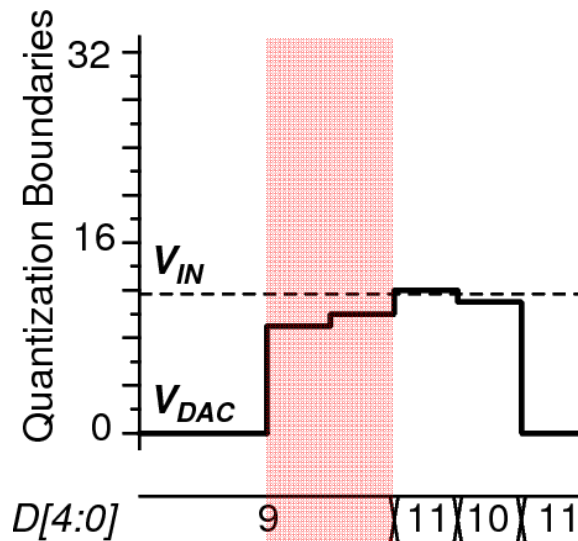
Bitcycle	$D[4:0]$	DIR
1	01011	0
2	01011	1



LSB-first SA: Good Case

$$D_{PREV} = 9, D_{OUT} = 11$$

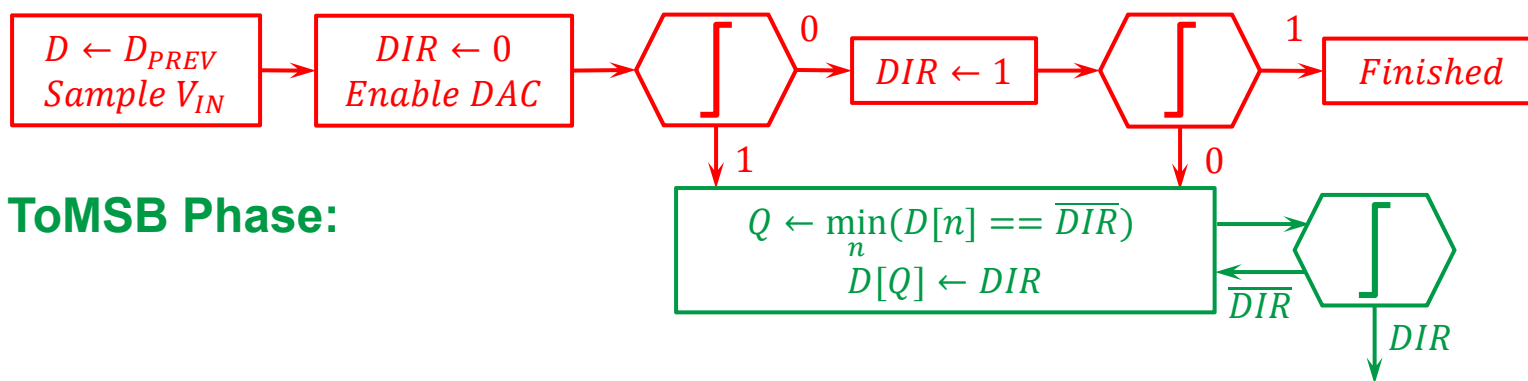
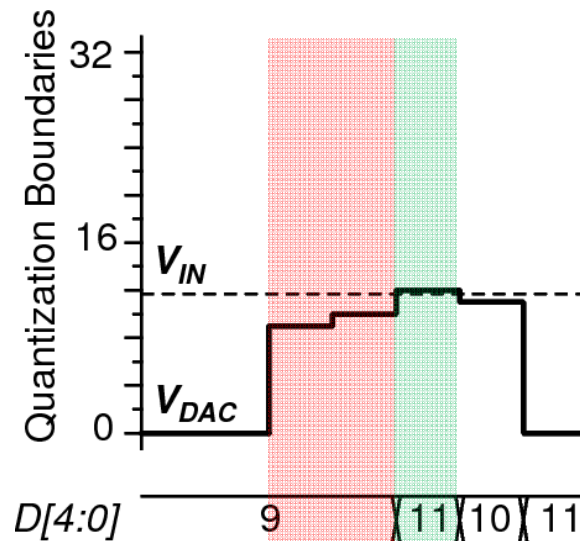
Bitcycle	$D[4:0]$	DIR
1	01001	0
2	01001	1
3	01011	1
4	01010	1



LSB-first SA: Good Case

$$D_{PREV} = 9, D_{OUT} = 11$$

Bitcycle	$D[4:0]$	DIR
1	01001	0
2	01001	1
3	01011	1
4	01010	1

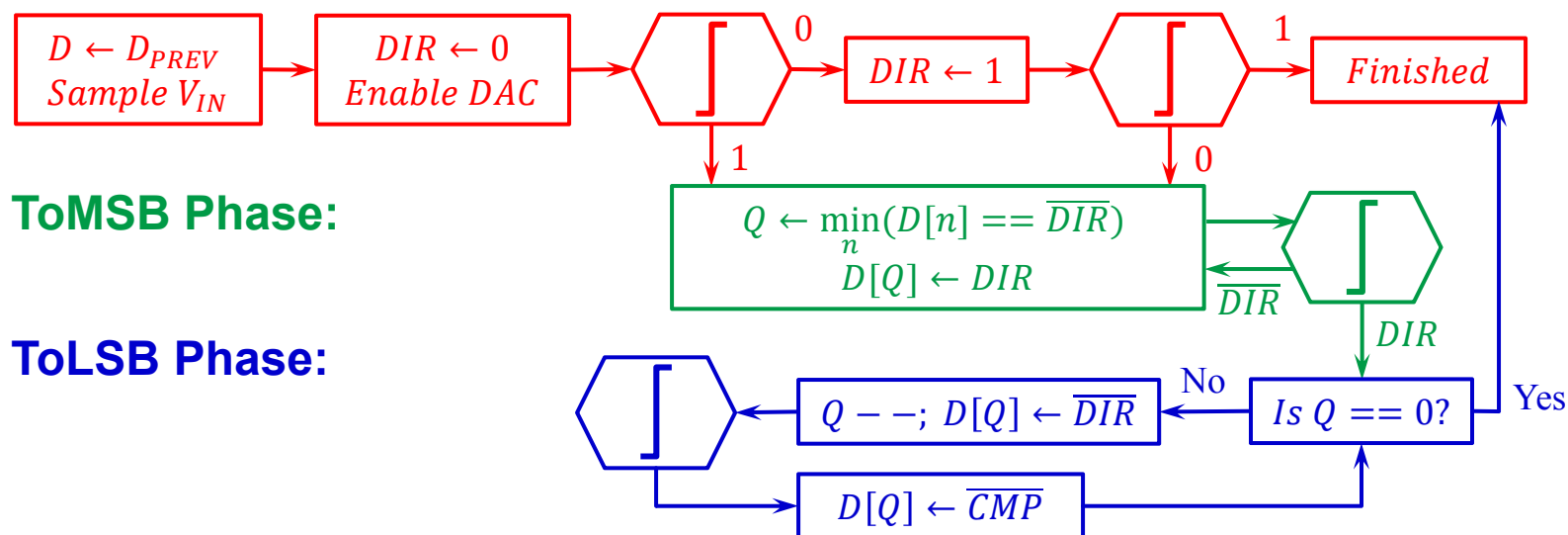
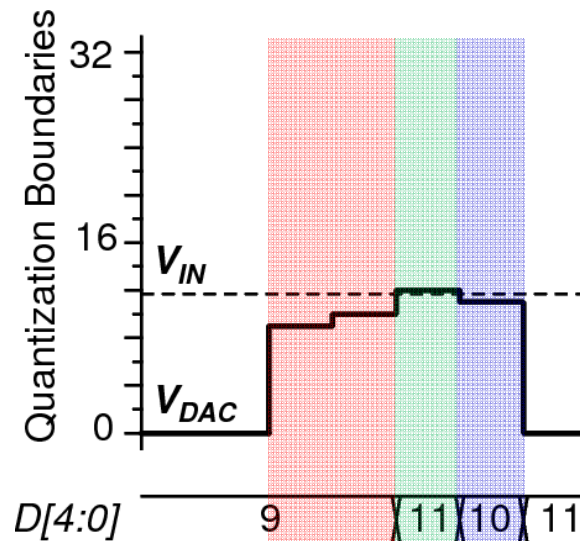


ToMSB Phase:

LSB-first SA: Good Case

$D_{PREV} = 9, D_{OUT} = 11$

Bitcycle	$D[4:0]$	DIR
1	01001	0
2	01001	1
3	01011	1
4	01010	1

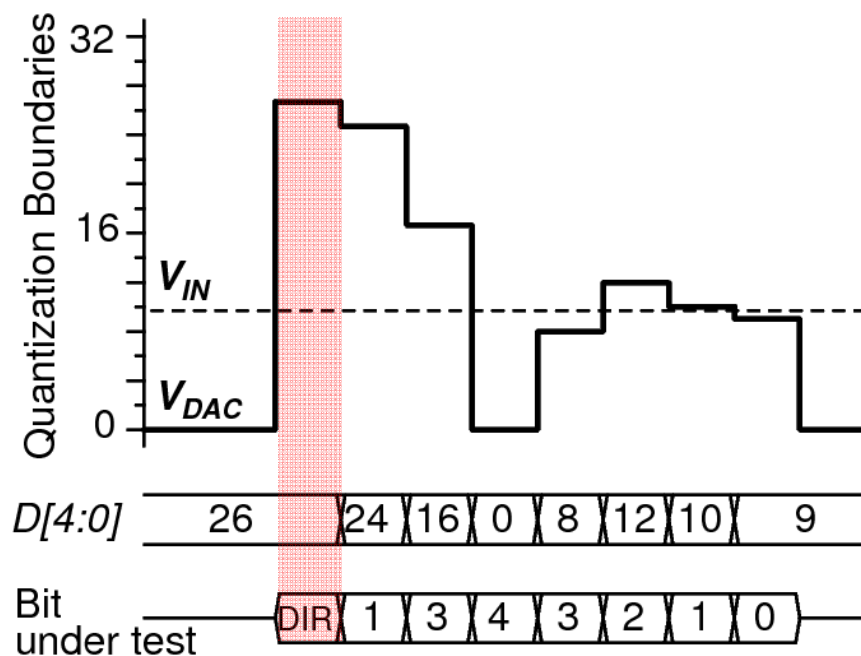


LSB-first SA: Bad Case

$$D_{PREV} = 26, D_{OUT} = 9$$

INIT

Bitcycle	$D[4:0]$	DIR
1	11010	0
2	11000	0
3	10000	0
4	00000	0
5	01000	0
6	01100	0
7	01010	0
8	01001	0

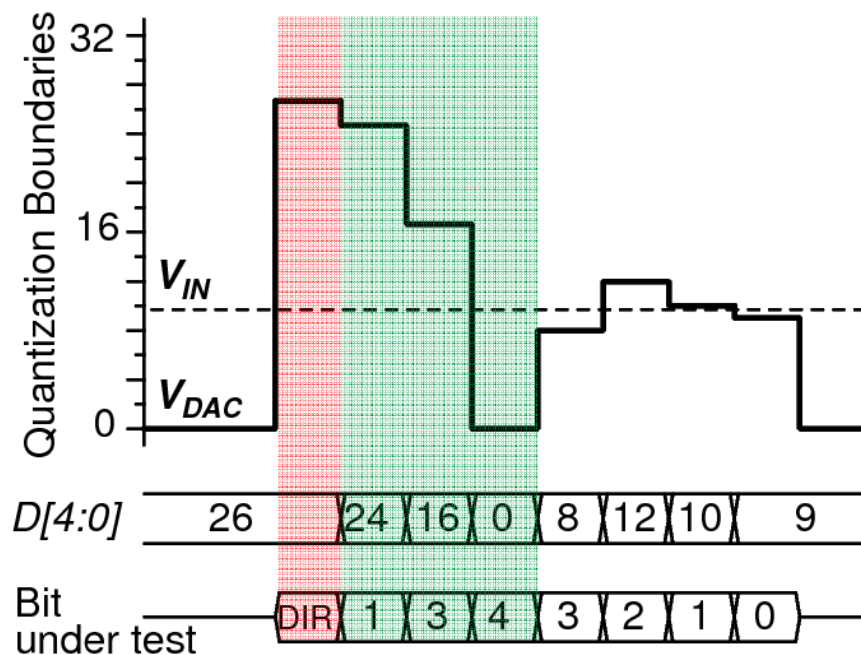


LSB-first SA: Bad Case

$$D_{PREV} = 26, D_{OUT} = 9$$

INIT
ToMSB

Bitcycle	$D[4:0]$	DIR
1	11010	0
2	11000	0
3	10000	0
4	00000	0
5	01000	0
6	01100	0
7	01010	0
8	01001	0



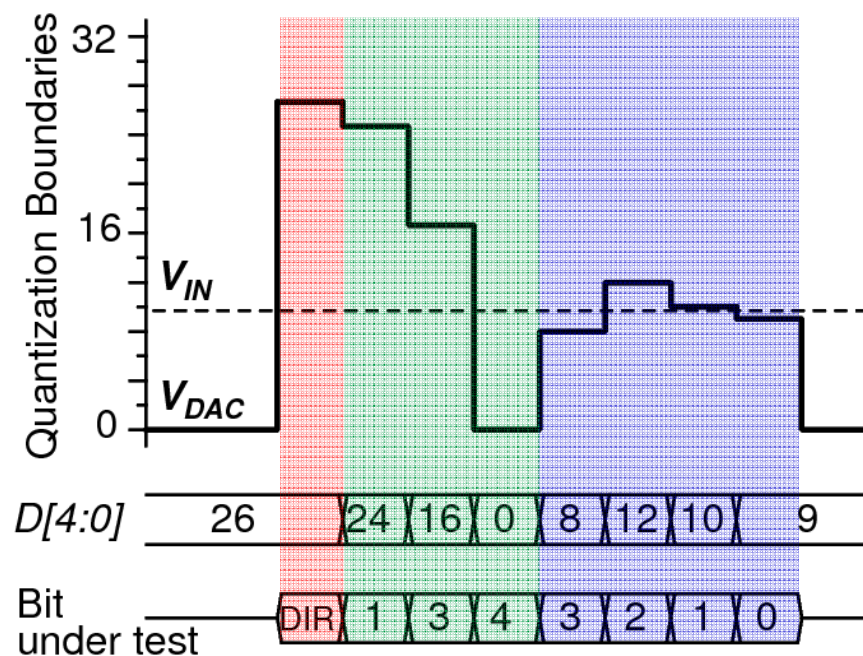
LSB-first SA: Bad Case

$$D_{PREV} = 26, D_{OUT} = 9$$

INIT
ToMSB

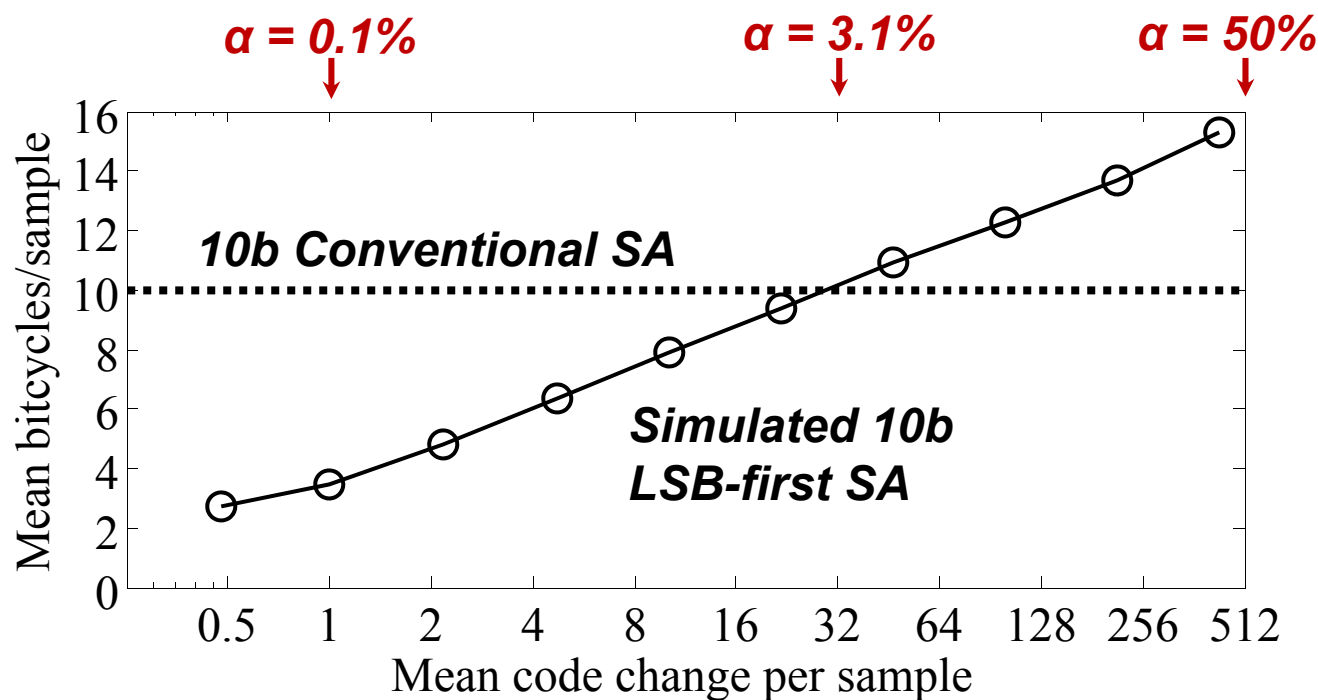
ToLSB

Bitcycle	$D[4:0]$	DIR
1	11010	0
2	11000	0
3	10000	0
4	00000	0
5	01000	0
6	01100	0
7	01010	0
8	01001	0



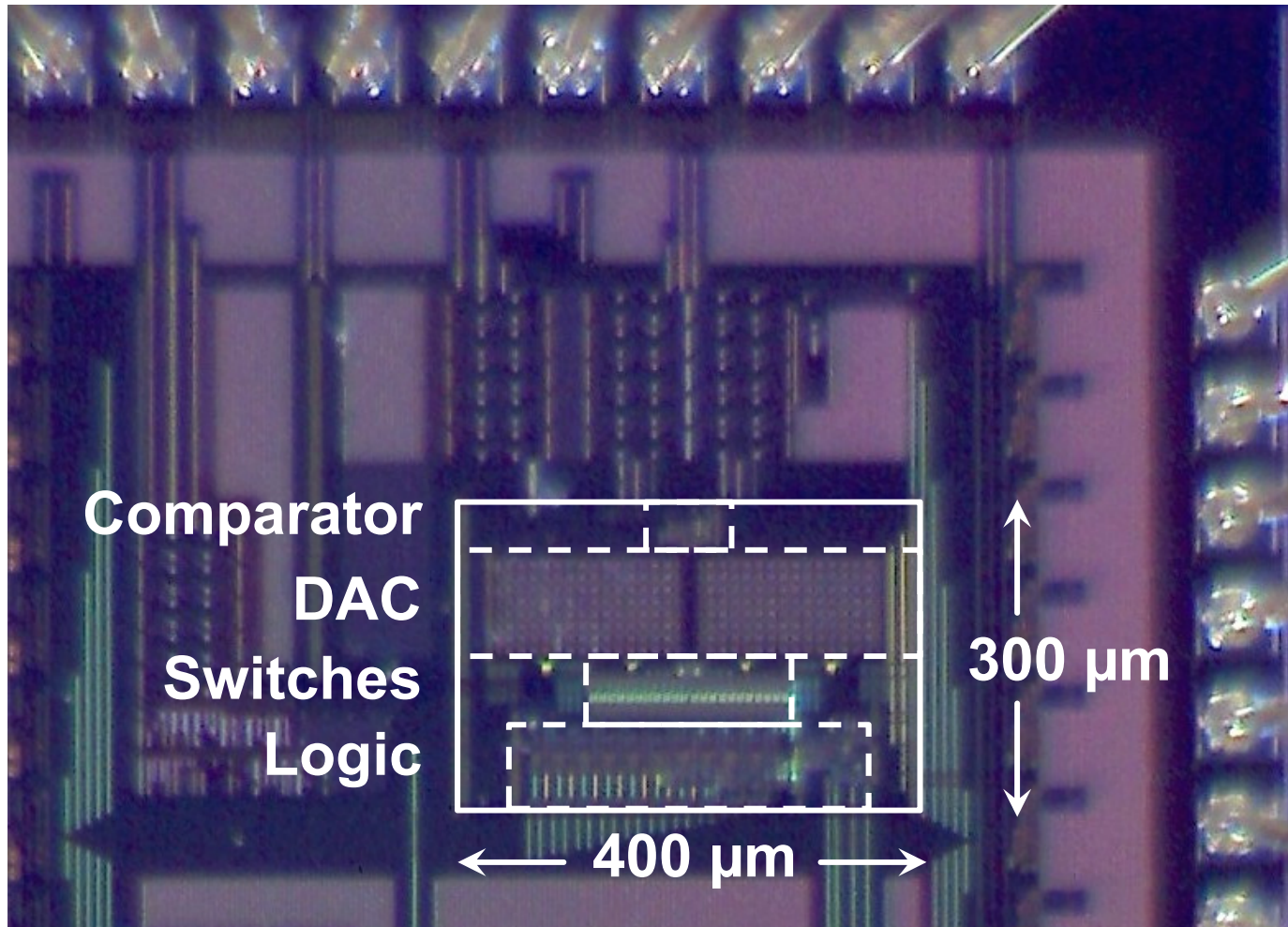
LSB-first SA Performance

- Uses between 2 and $2N+1$ bitcycles for an N -bit conversion
- Simulate performance for fullscale sinusoid inputs of different frequencies



Bitcycles/sample **scales logarithmically** with initial guess error (code change magnitude)

ADC Test Chip



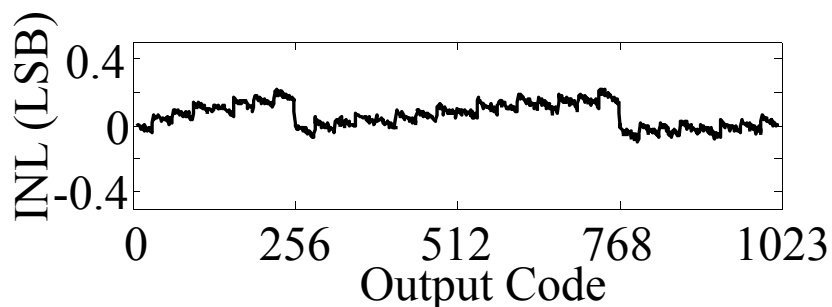
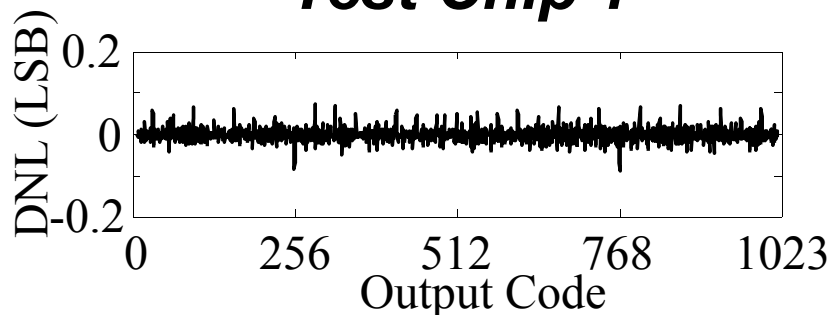
0.18 μm General Purpose CMOS

11.3: A 10b 0.6nW SAR ADC with Data-Dependent
Energy Savings Using LSB-first Successive Approximation

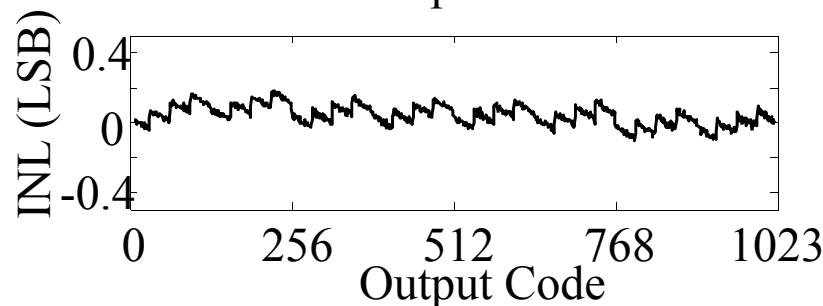
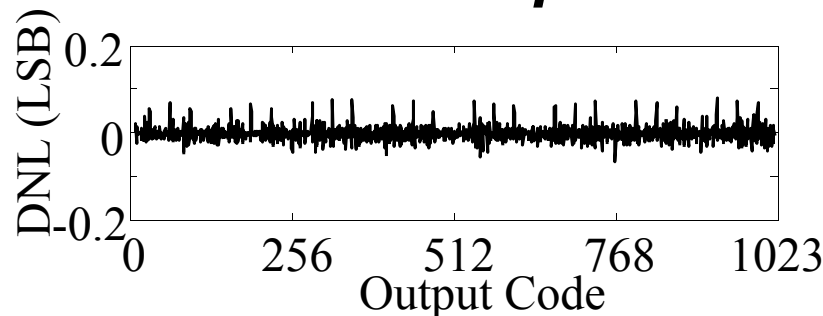
Static Linearity Measurements

- Low-frequency Sinusoid Histogram Test
- 0.1 LSB ripple with 32 code period due to C_C mismatch

Test Chip 1



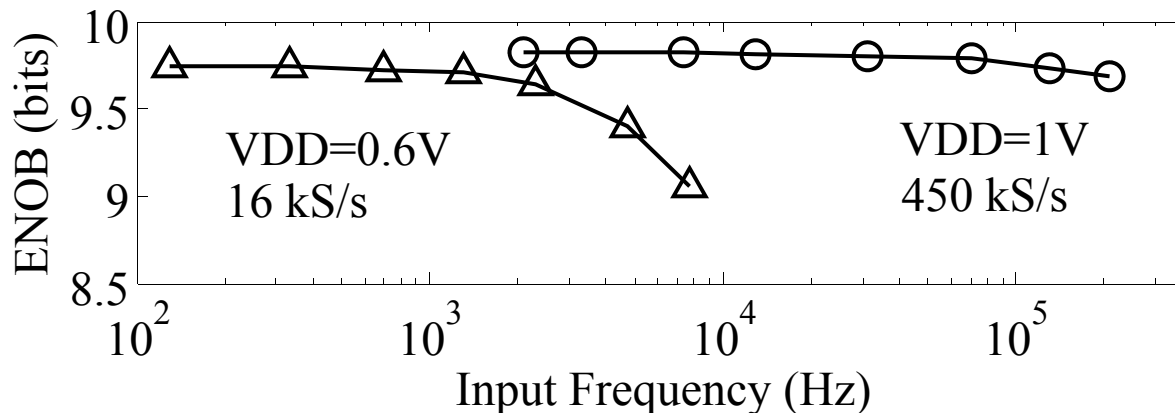
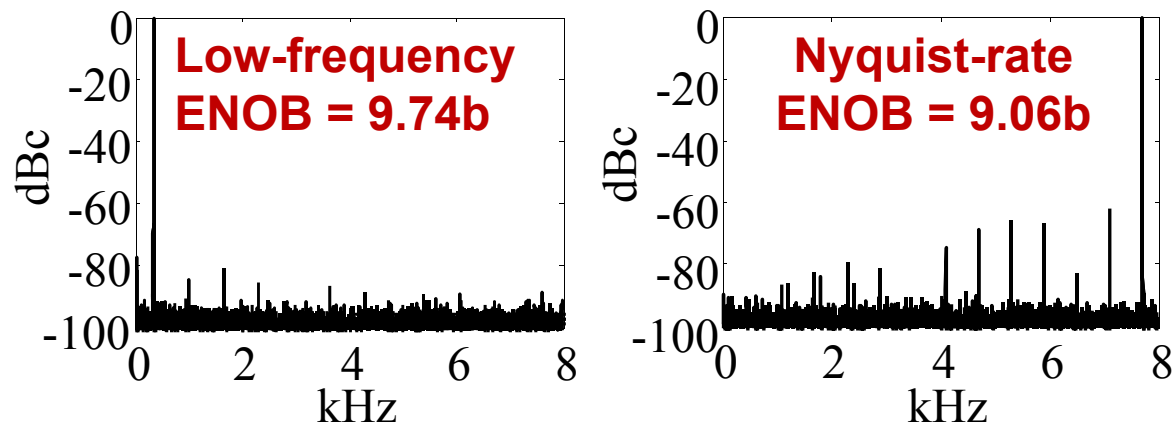
Test Chip 3



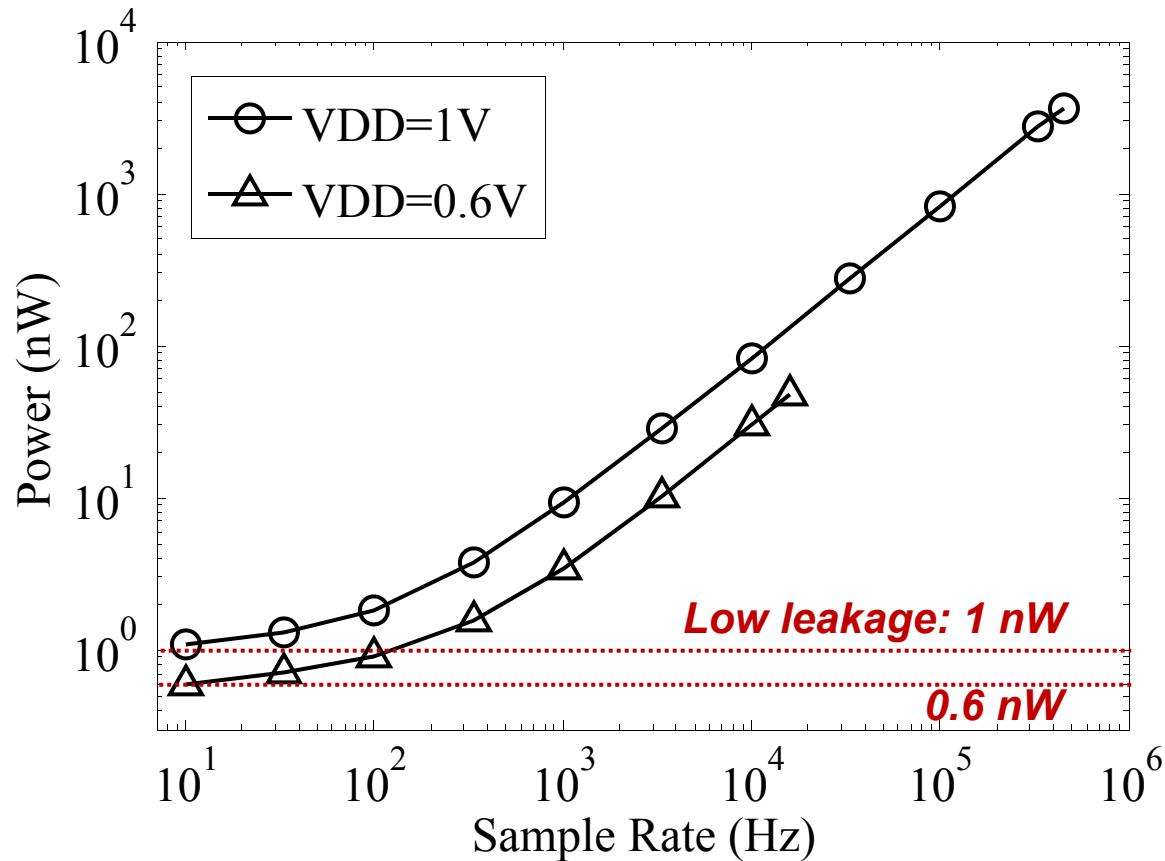
DNL/INL bounded at +0.1/-0.1 LSB and +0.22/-0.14 LSB over 10 test chips

Spectral Measurements

***ENOB hurt by sampling switch resistance
at $V_{DD} = 0.6V$, $f_s = 16 \text{ kS/s}$***

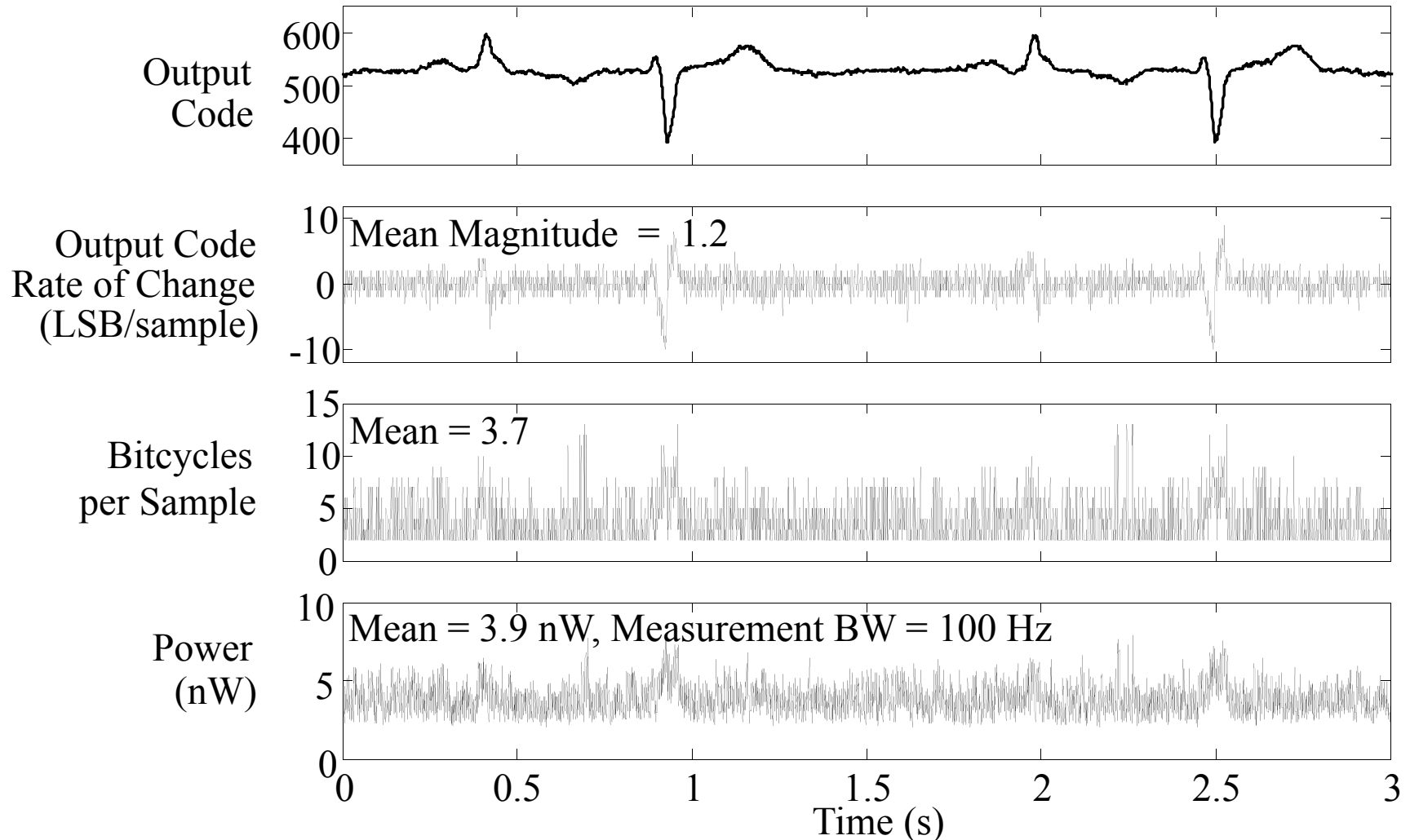


Sample Rate and Power Consumption



Fixed sample rate $f_s \leq f_{CLK}/25$ accommodates worst-case bitcycles/sample of $2N+1$

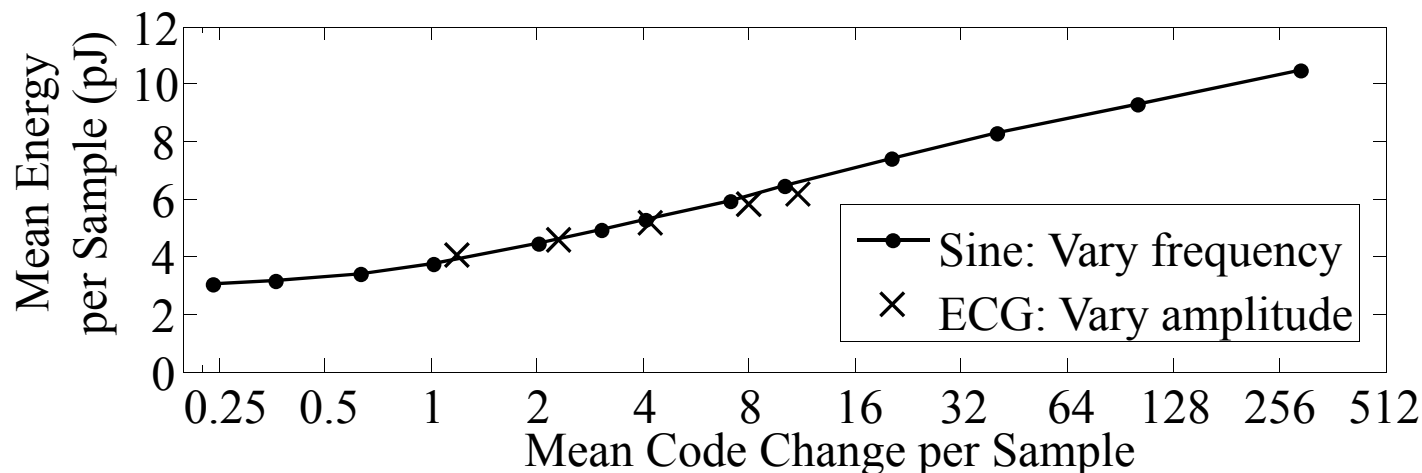
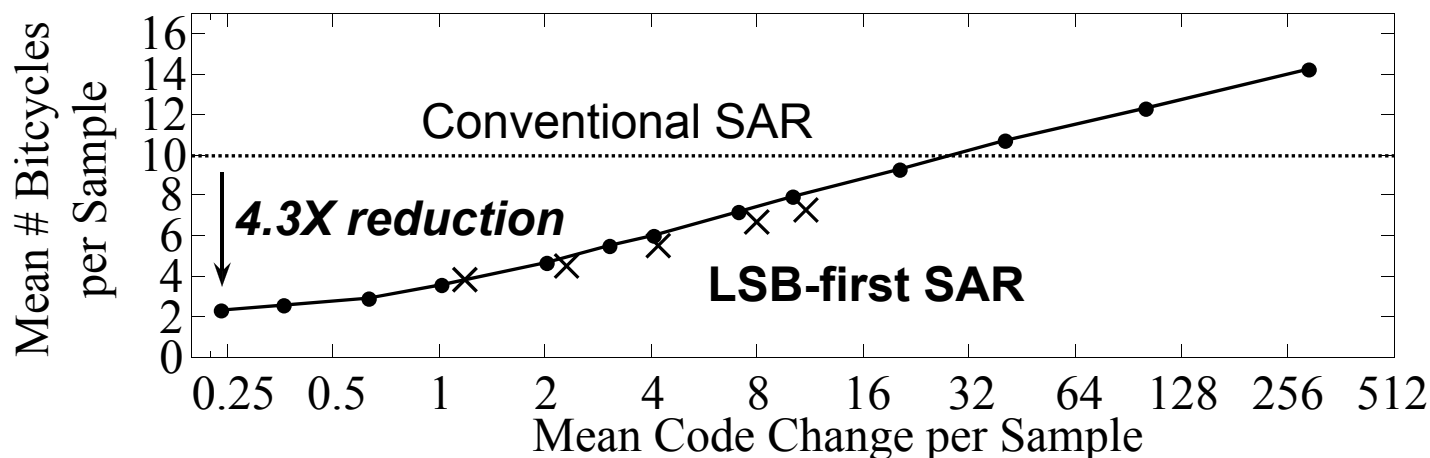
Electrocardiogram Test Input



ADC response to ECG test input signal at $V_{DD}=0.5V$ and $f_s=1\text{ kHz}$

Data-dependent Power Consumption

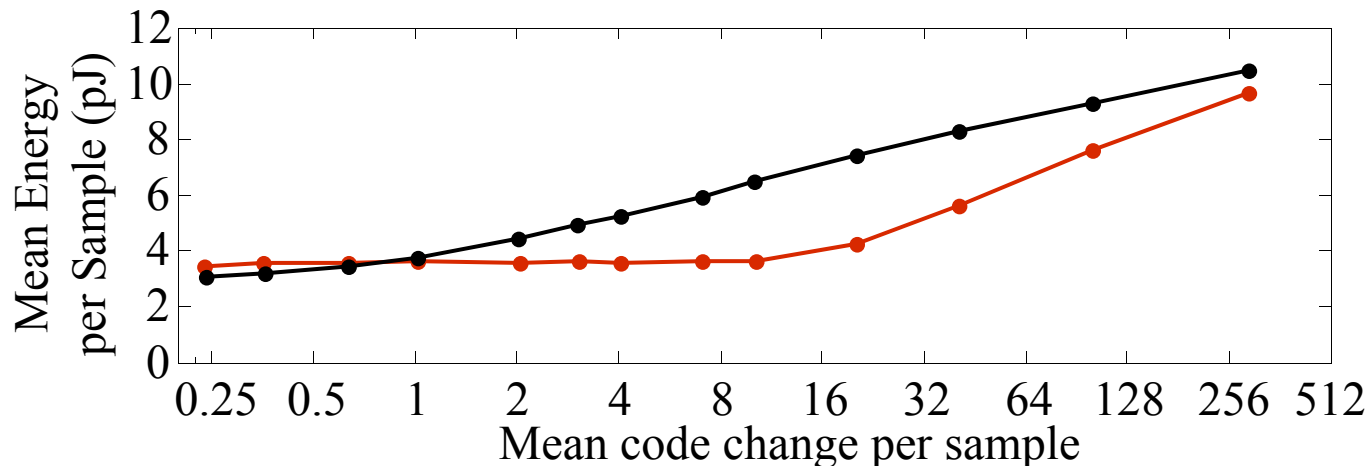
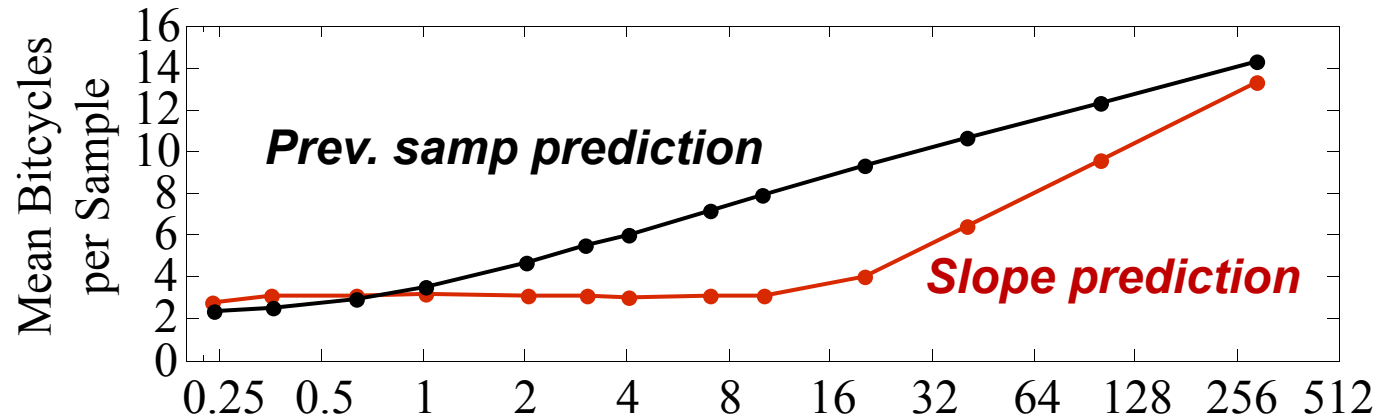
Measured ADC performance at $V_{DD}=0.6V$ and $f_S=10\text{ kHz}$



Estimate ADC performance for arbitrary signals using $\langle \Delta code \rangle$

Externally Computed Prediction

- First-order linear prediction works well for smooth signals
- $D_{N,guess} \leftarrow D_{N-1} + (D_{N-1} - D_{N-2})$



ADC Performance Summary

Comparison with recent low-leakage 10b SAR ADC designs:

	[1]	[2]	[3]	This Work		
Technology	65nm	0.18 μ m	65nm	0.18 μ m		
Area (mm²)	0.212	0.082	0.076	0.12		
Unit Capacitor (fF)	65	4.5	0.25	72		
Supply Voltage (V)	0.55	0.6	0.6	1.0	0.6	0.5
Sample Rate (Hz)	20k	200k	40k	450k	16k	4k
ENOB (bit)	8.84	9.34	9.4	9.82	9.73	9.55
Power (W)	206n	1.04 μ	72n	3.7–13 μ	47–170n	8.7–31n
FoM (fJ)	22.4	8.03	2.7	9.1–35	3.5–20	2.9–17

[1] M. Yip, A. Chandrakasan, *ISSCC 2011*

[2] G. Y. Huang et al., *JSSC 2012*

[3] P. Harpe et al., *ISSCC 2013*

**Range is given for best case (DC)
and worst case (fullscale Nyquist
sinusoid) inputs.**

Conclusion

LSB-first Successive Approximation ...

- Uses fewer bitcycles with good initial guess
- Nearly drop-in replacement for conventional SAR
- Power scales smoothly with signal activity
- Maintains constant rate/resolution

Acknowledgements:

NDSEG Fellowship, TSMC University Shuttle Program, Shell and Texas Instruments, and M. Yip.

A 1.5mW 68dB-SNDR 80MS/s 2-times interleaved SAR-assisted pipelined ADC in 28nm CMOS



Session 11.4

February 11, 2014

**Frank van der Goes, Chris Ward, Santosh Astgimath¹, Han Yan,
Jeff Riley, Jan Mulder, Sijia Wang and Klaas Bult**

Broadcom Netherlands, ¹ now at Wolfson Microelectronics, Scotland

Summary

80MS/s 11-bit ENOB ADC

Industrial Environment

Embedded Application

Goal: Lowest Power

Summary

80MS/s 11-bit ENOB ADC

Industrial Environment



on-chip circuits:

- **Reference Generator**
- **Clock circuits**
- **Bias blocks**
- **Encoder**

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- Reduced ADC Full-scale to allow on-chip driver
→ Max input: $1.4 V_{ppd}$
- 28nm standard CMOS

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80MS/s 11-bit ENOB ADC

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Embedded Application



- **Reduced ADC Full-scale to allow on-chip driver**
→ **Max input: $1.4 V_{ppd}$**
- **28nm standard CMOS**

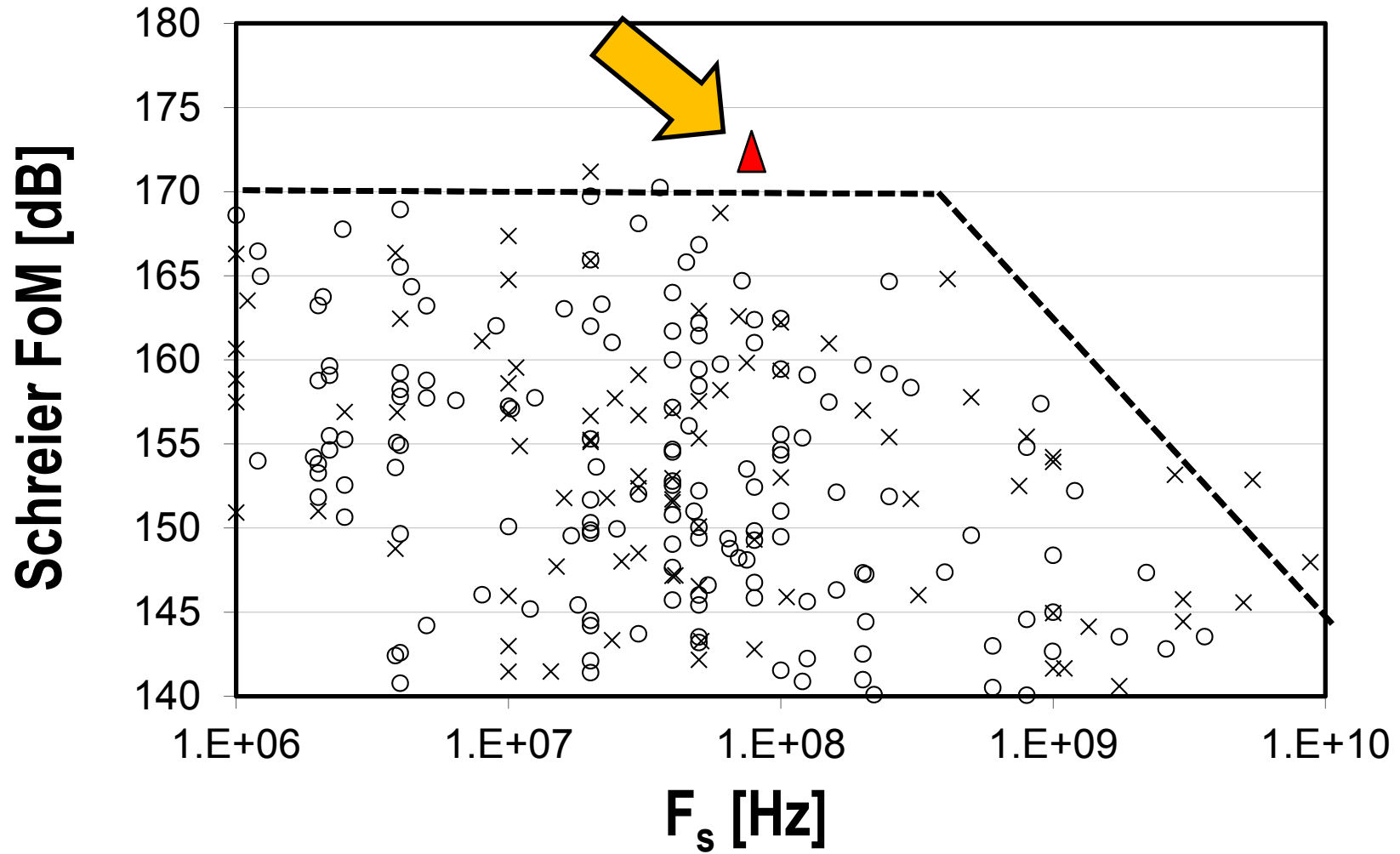
Goal: Lowest Power



Power: 1.5mW

Power Efficiency, ISSCC / VLSI, 1997-2013

B. Murmann, ADC survey , July 2013



Schreier FoM: Widely used for Noise-Limited designs

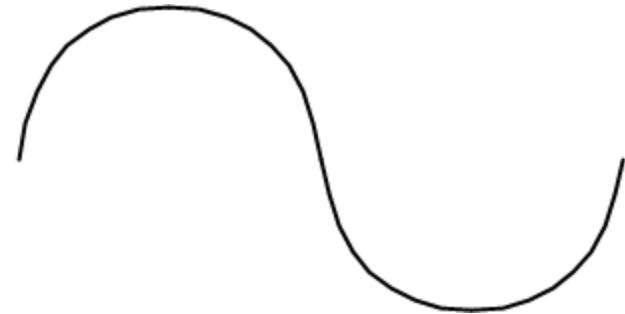
Improving Power Efficiency

Noise



- **ADC Architecture**
- **Noise Filtering using Integrators**

Large Signals



- **Reference Settling**
- **Reduced DAC Switching Energy**

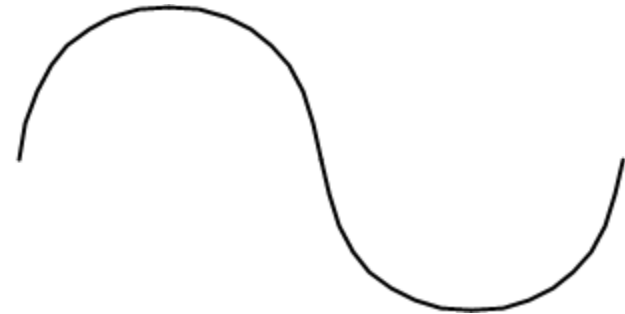
Improving Power Efficiency

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ADC Architecture

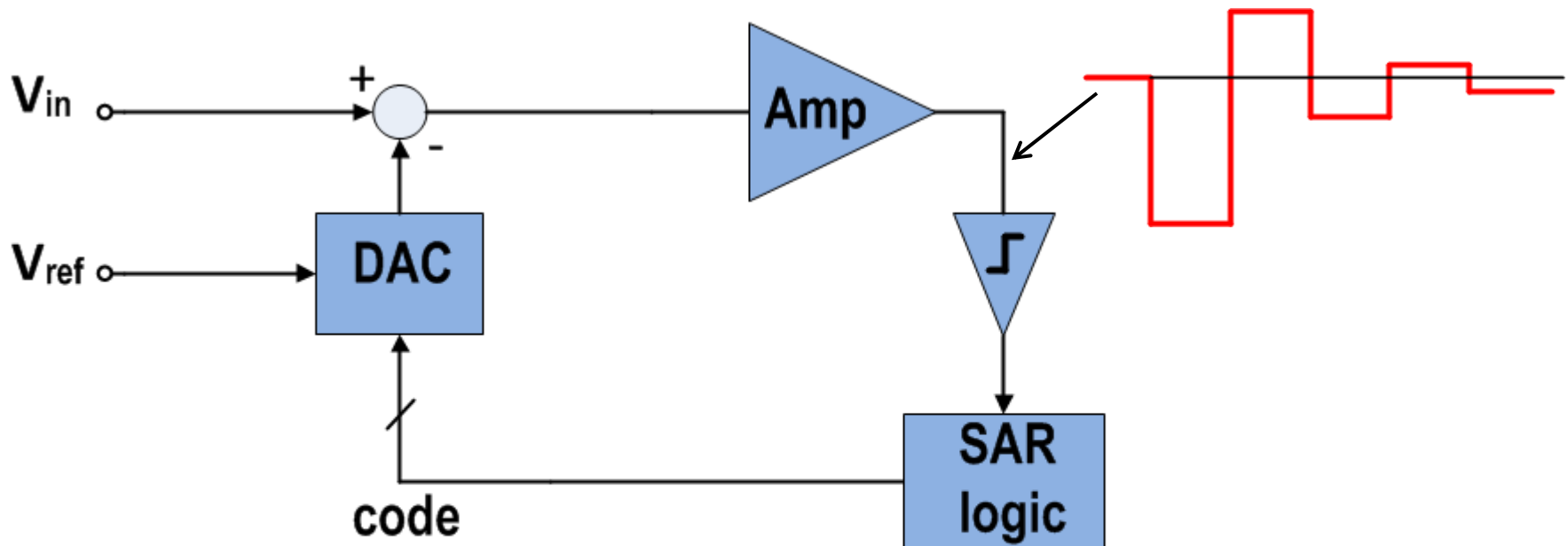
SAR-assisted pipelined ADC

– Lee [VLSI 2010]

Pipelining → good power-efficiency for noise

SAR ADC → good power-efficiency for large signals

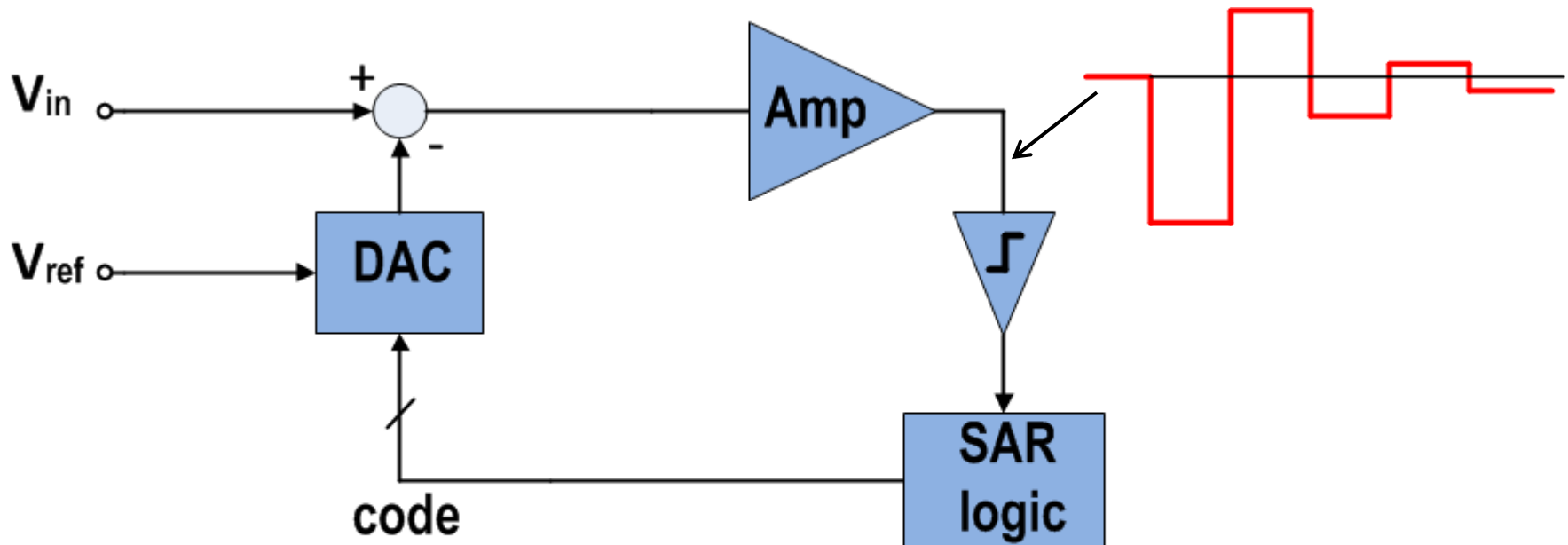
A SAR ADC



Noise-limited design: add amplifier

How much energy is spent to bring down the noise level ?

A SAR ADC

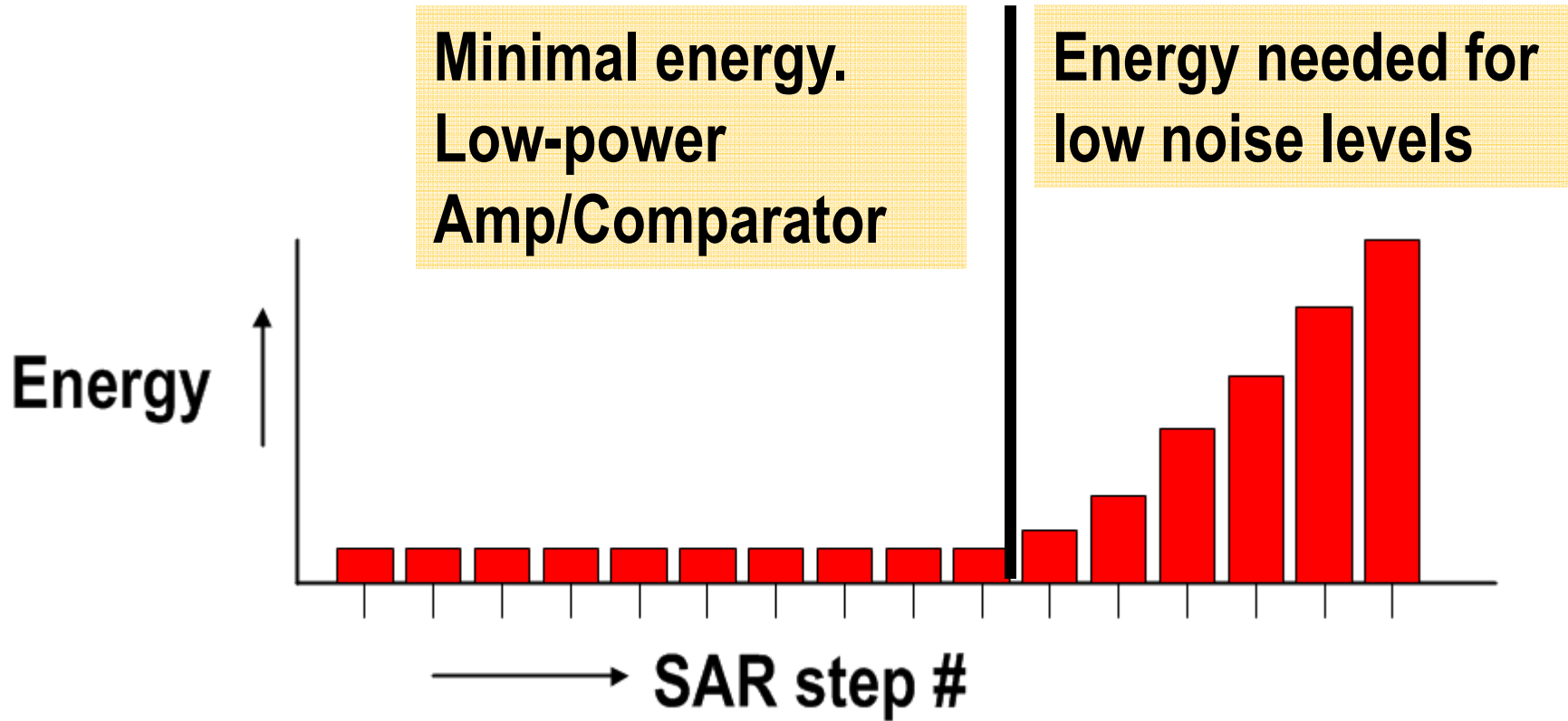


Low noise levels not needed during FIRST SAR steps

– Error correction applied, radix < 2

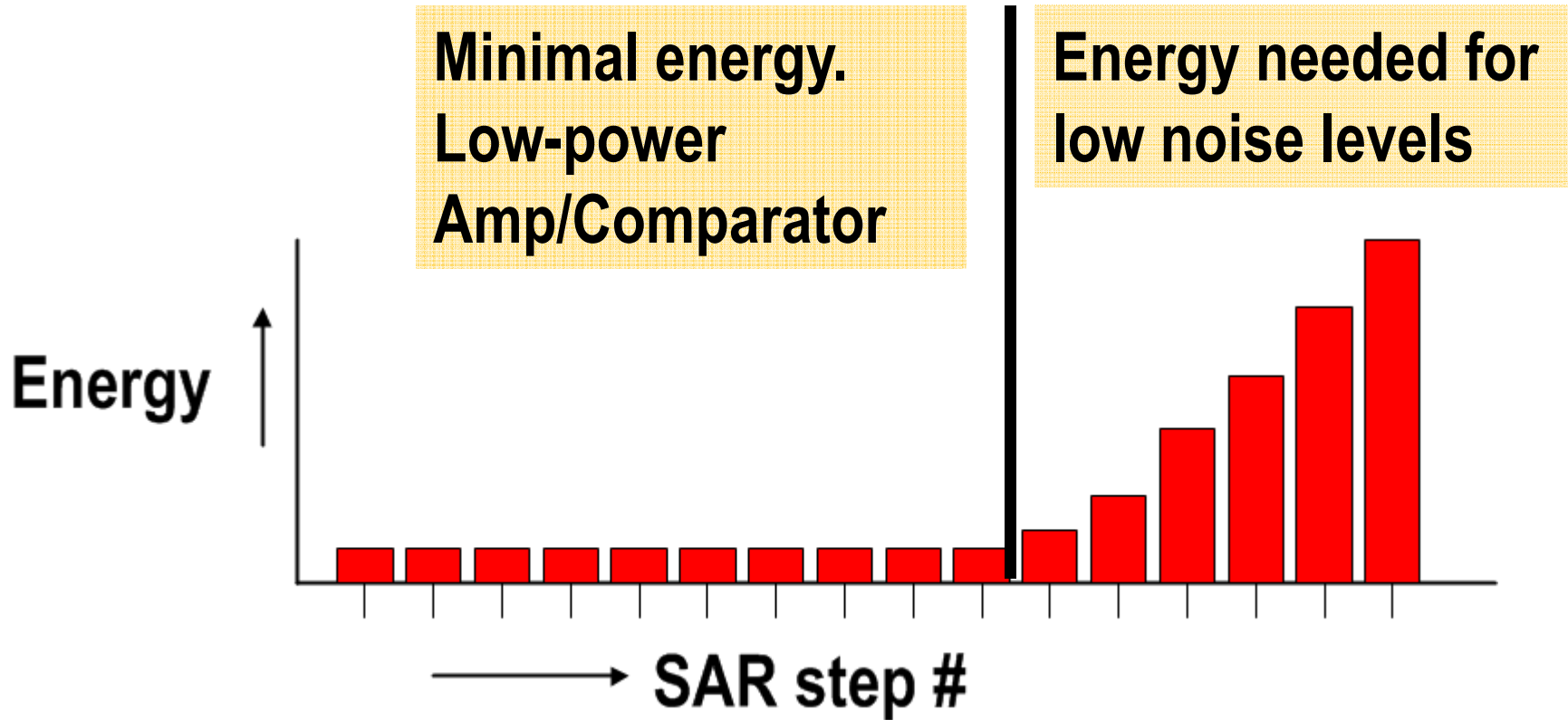
Low noise levels ONLY required during LAST SAR steps

Required Energy to bring down Noise Level



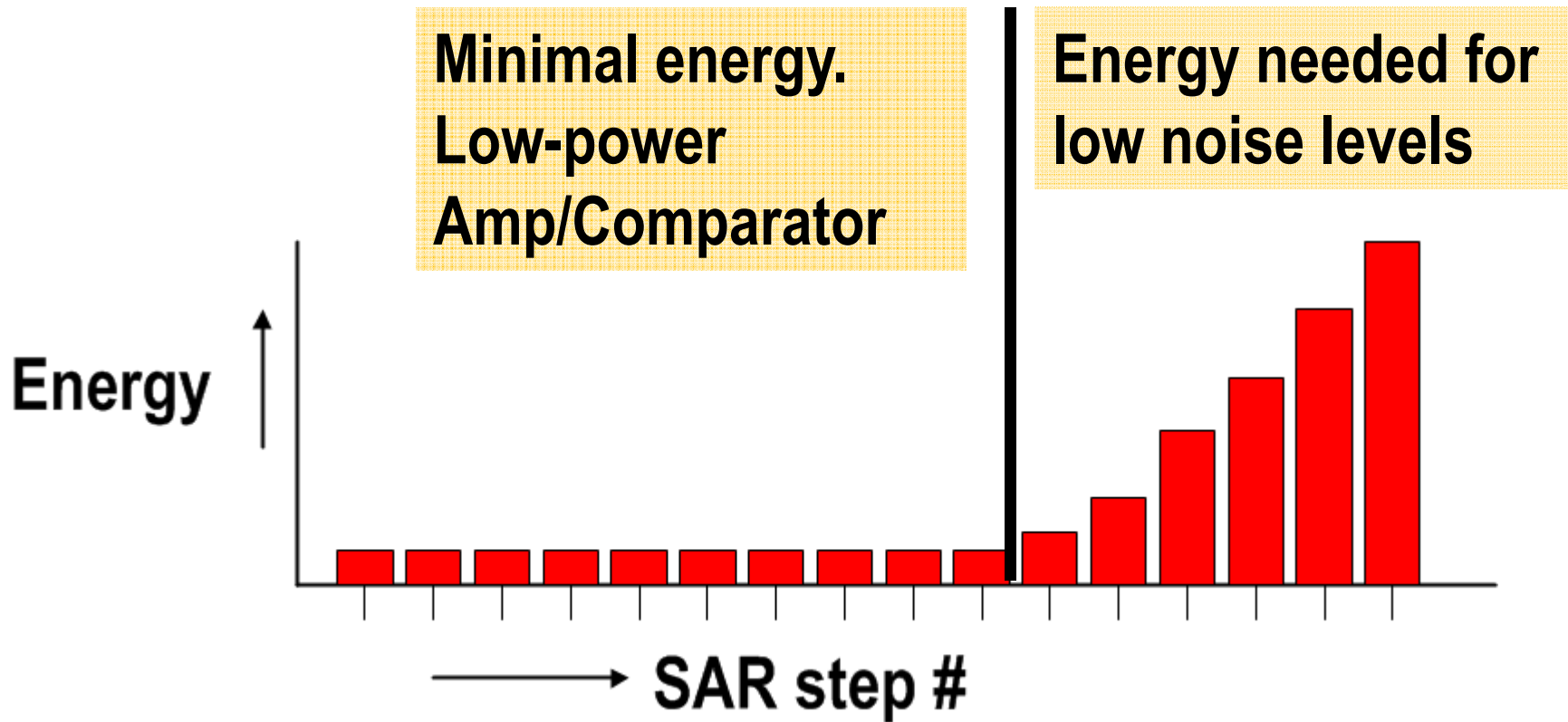
**DAC switching energy
is not considered here**

Required Energy to bring down Noise Level



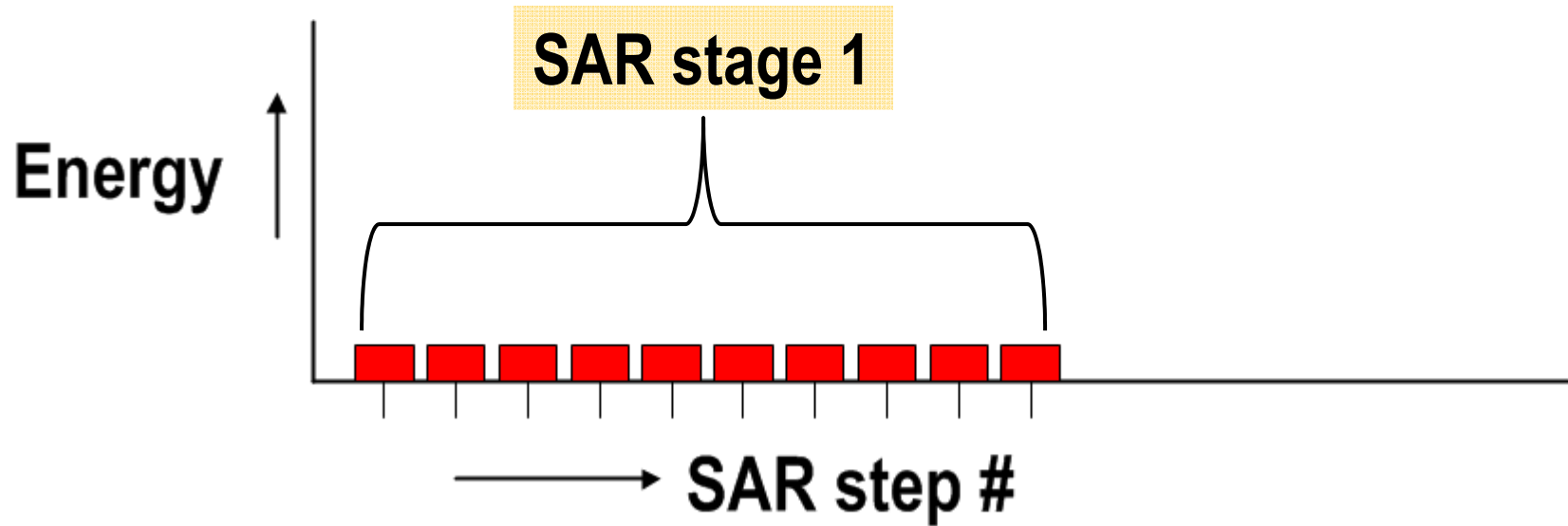
Multiple high-energy (low-noise) events

Required Energy to bring down Noise Level

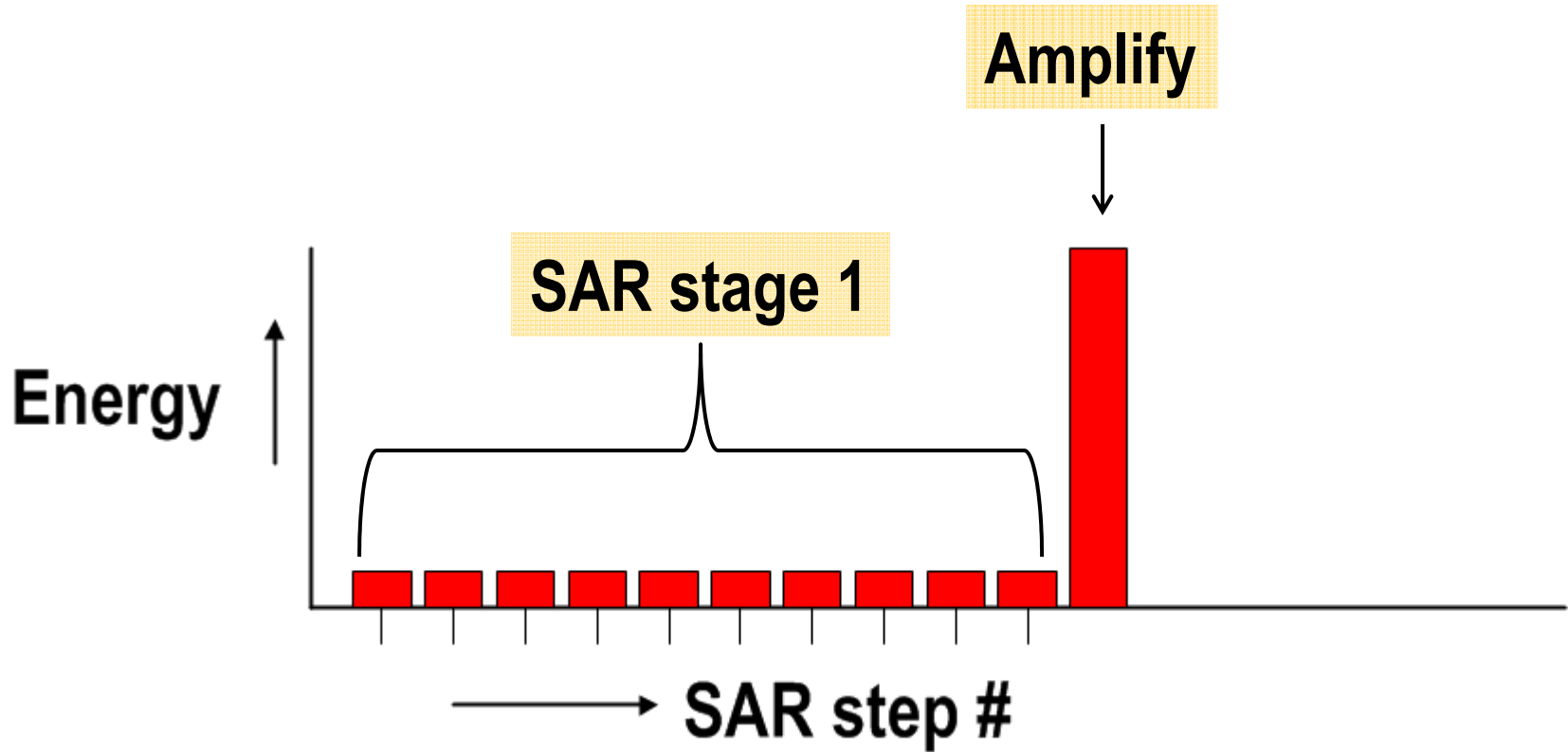


Multiple high-energy (low-noise) events
SAR-assisted pipelined ADC can do better !

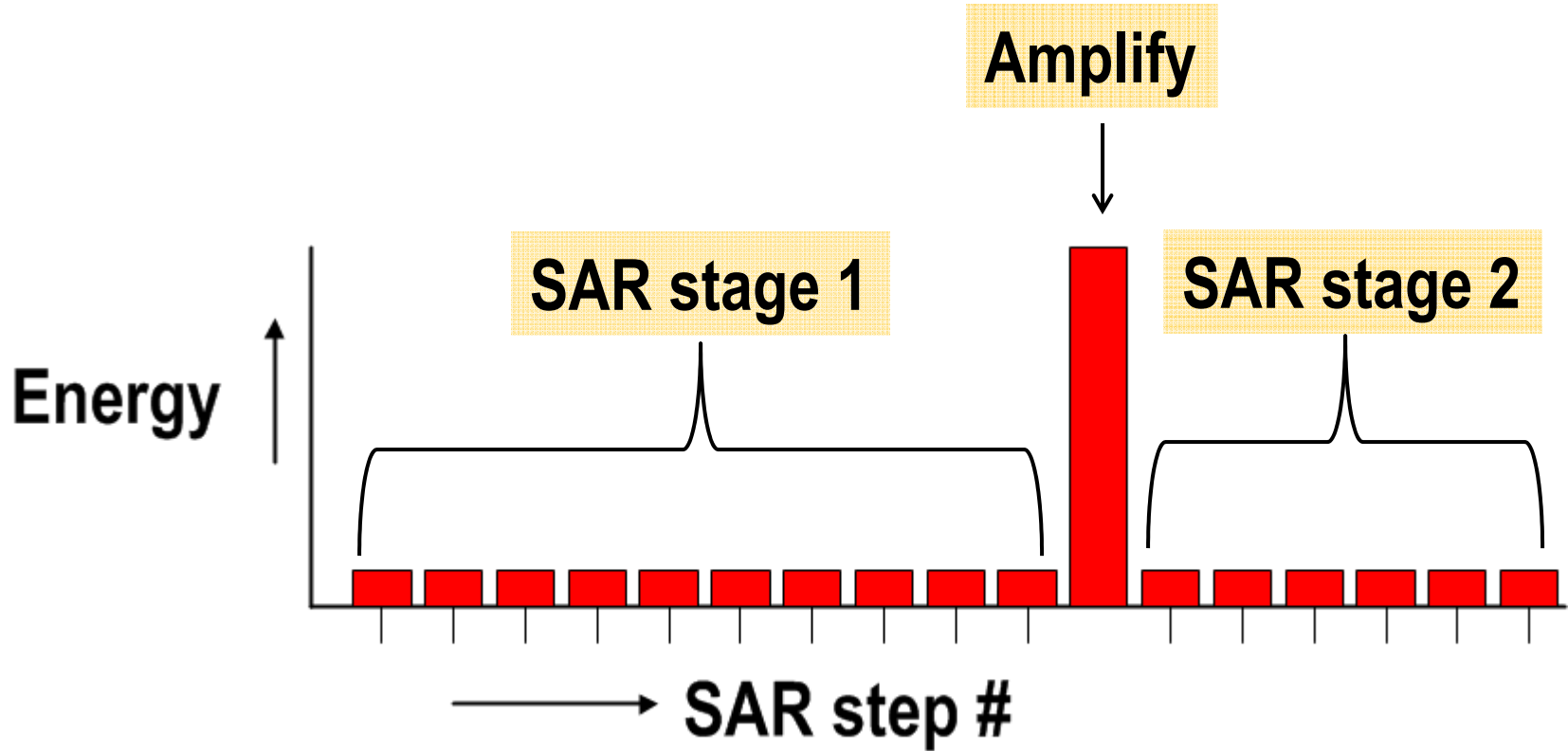
Required Energy of SAR-assisted Pipelined ADC



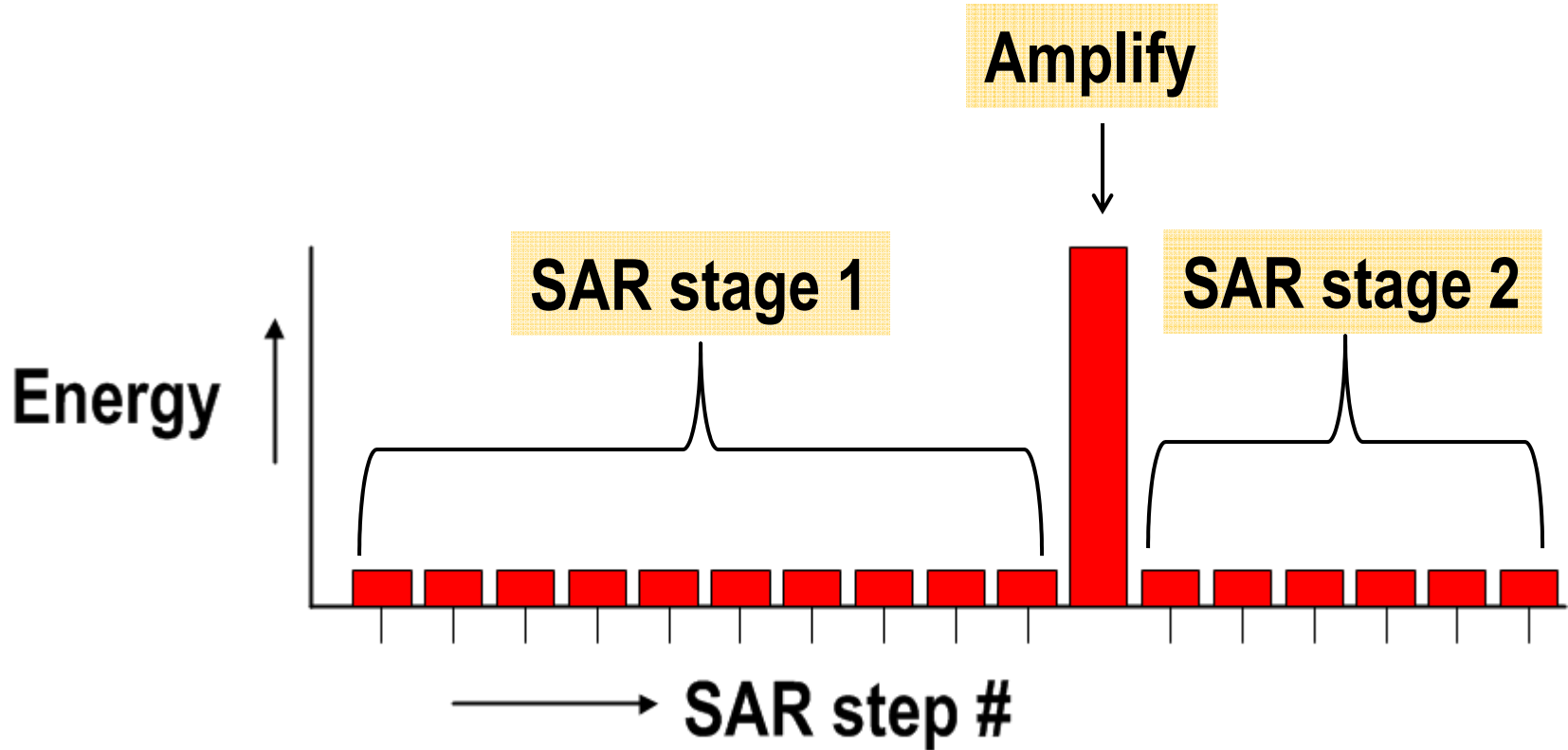
Required Energy of SAR-assisted Pipelined ADC



Required Energy of SAR-assisted Pipelined ADC

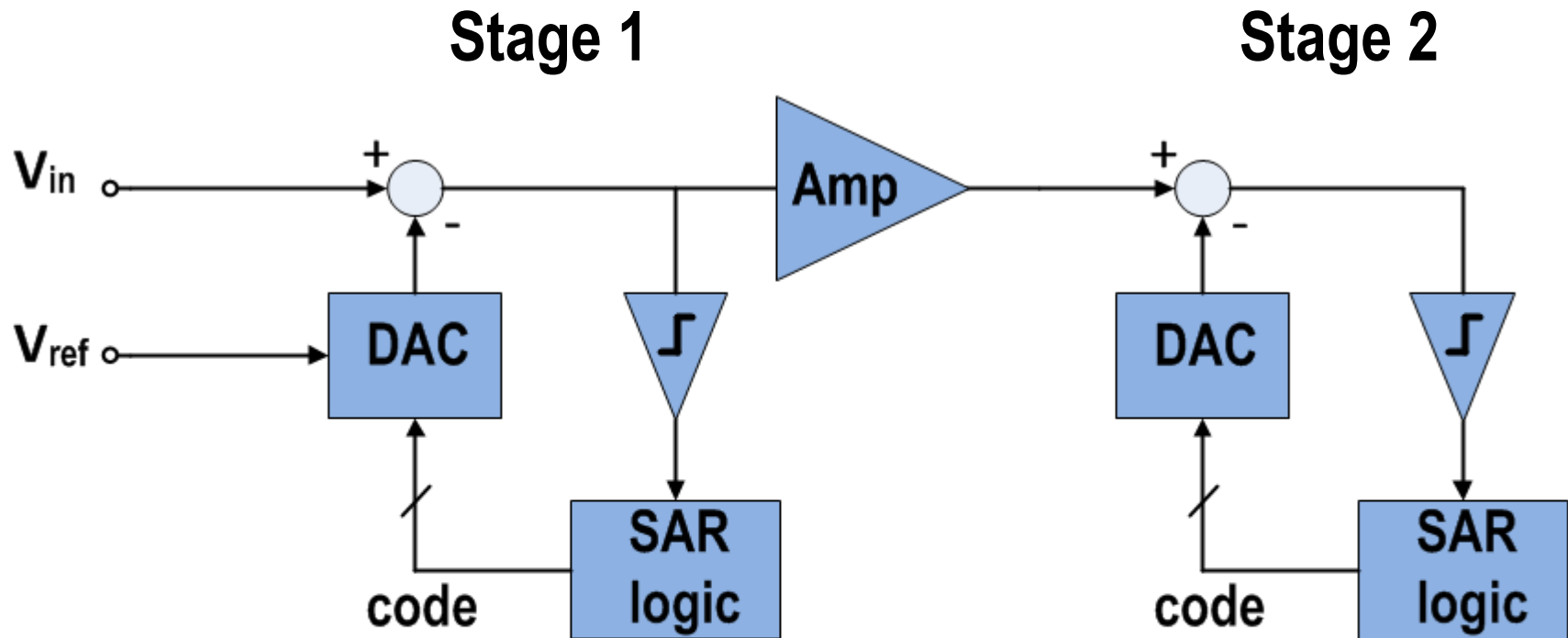


Required Energy of SAR-assisted Pipelined ADC

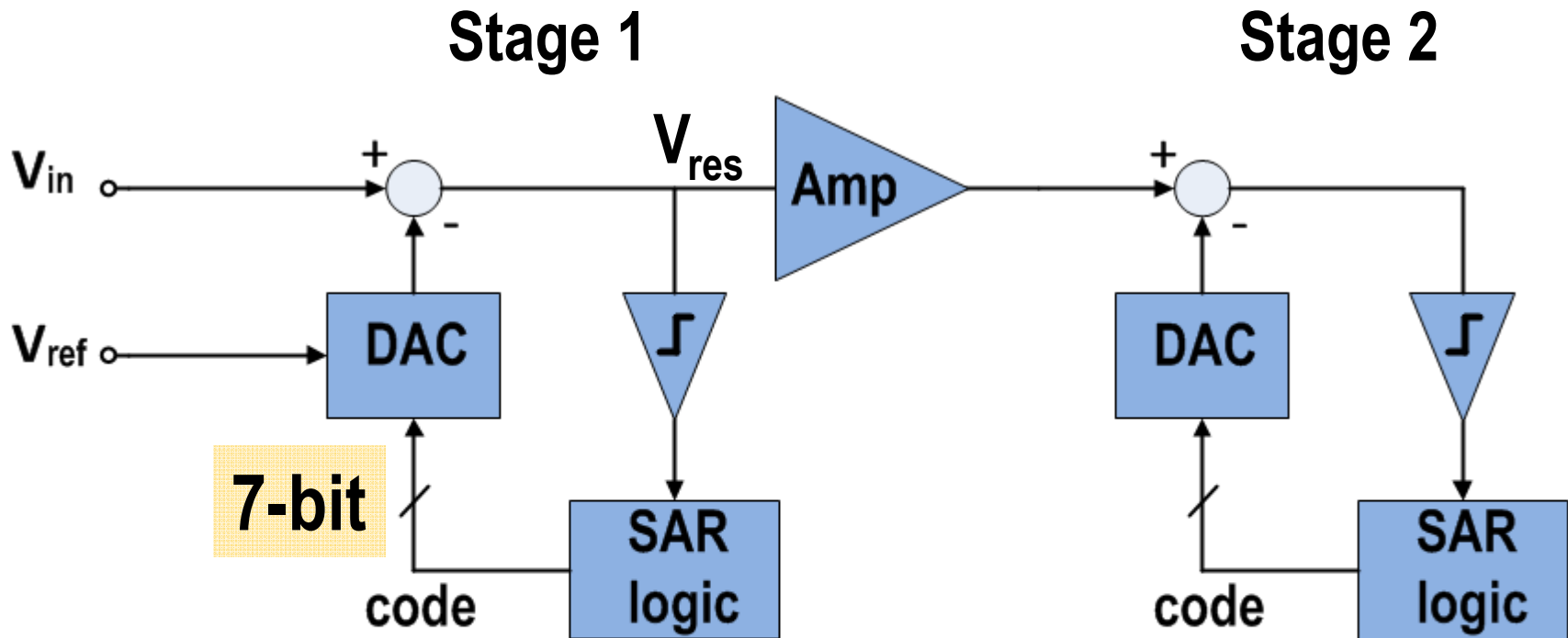


Low noise level is required only once
1 high-energy event: increased power efficiency wrt SAR

ADC Block Diagram



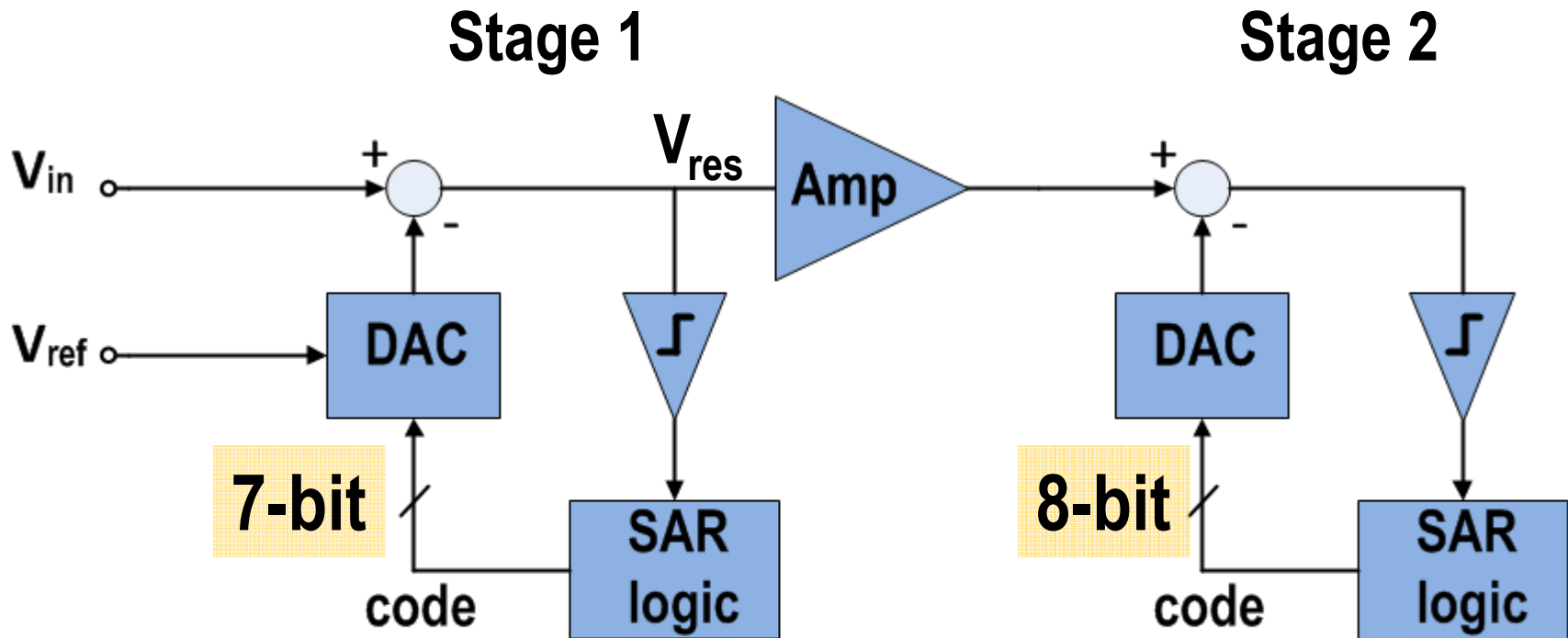
Resolution of Stage 1



Resolution Stage 1 optimized to 7 bits:

- Quantization steps $>$ noise of low-power comparator
- Small V_{res} : amplifier can be optimized for noise

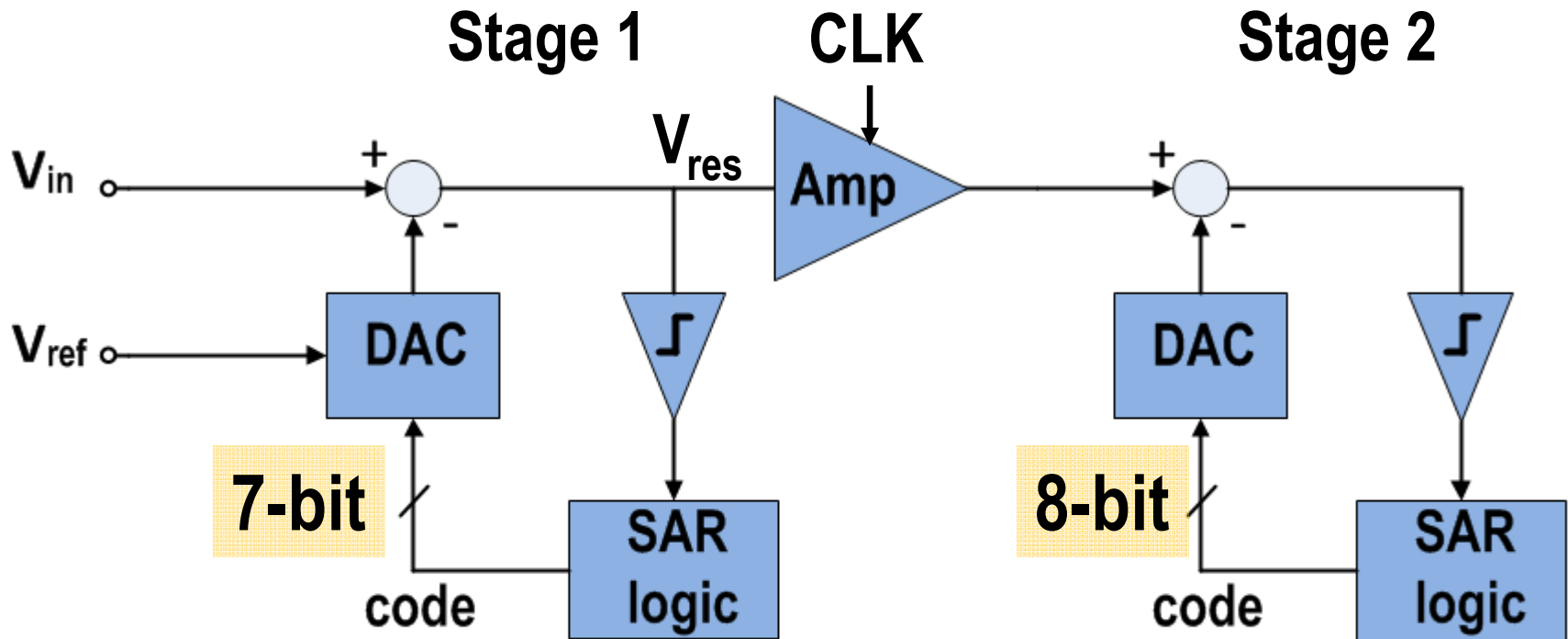
Resolution of Stage 2



Resolution Stage 2 set to 8 bits:

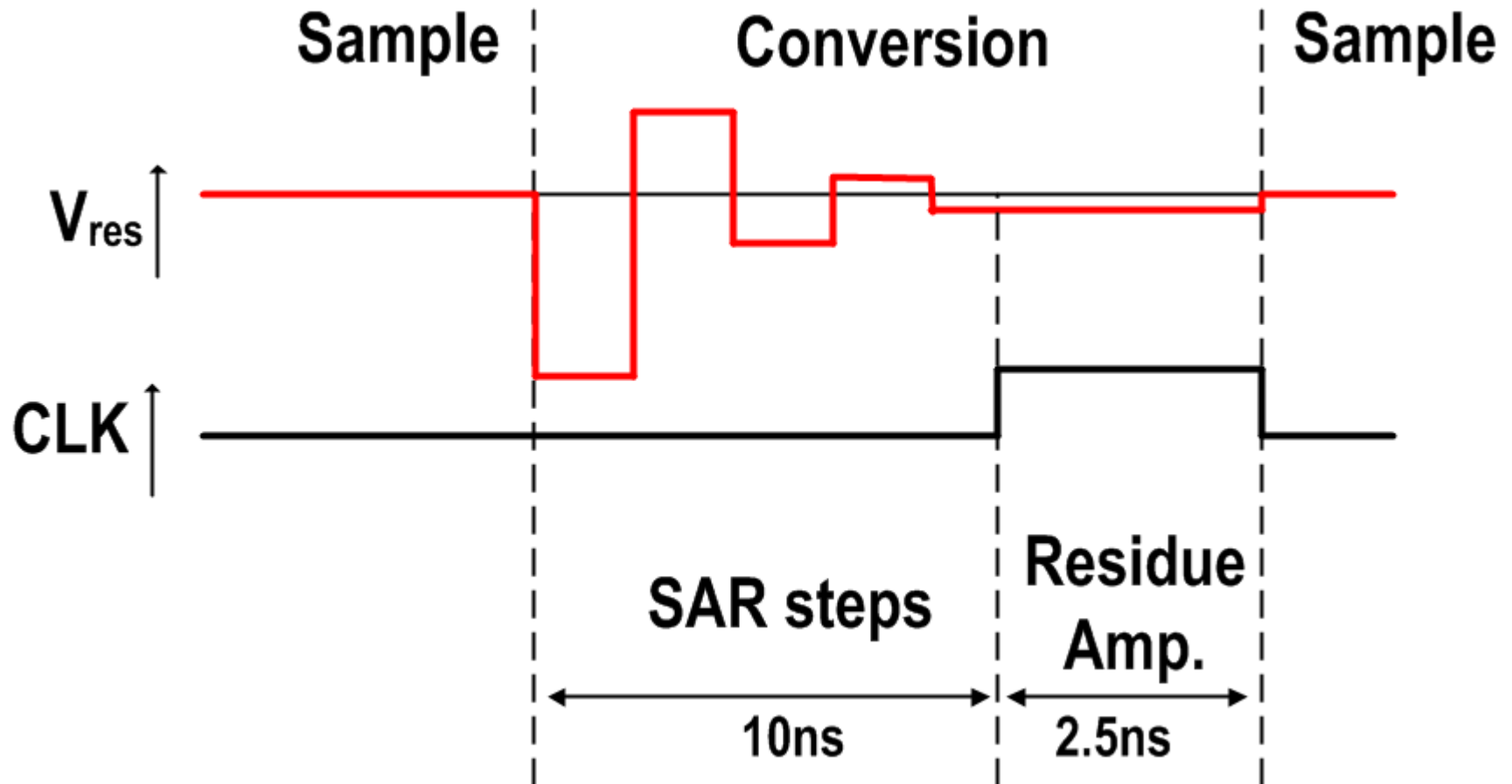
- Noise budget for quantization: 14 bit level
- 1 bit overrange between stage 1 and 2

SAR-assisted Pipelined ADC



- Dynamic Amplifier → switched OFF when not needed
- Amplifier gain: 16x

Residue Voltage



Residue Amplifier switched ON when SAR is DONE

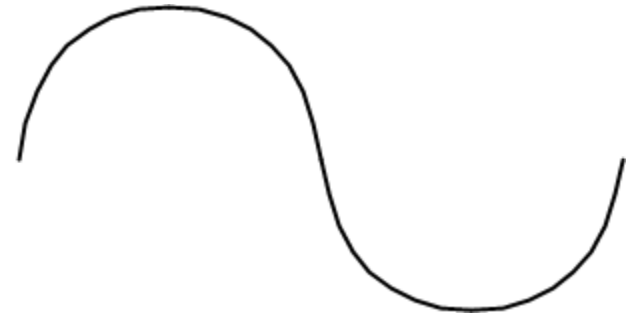
Improving Power Efficiency

Noise



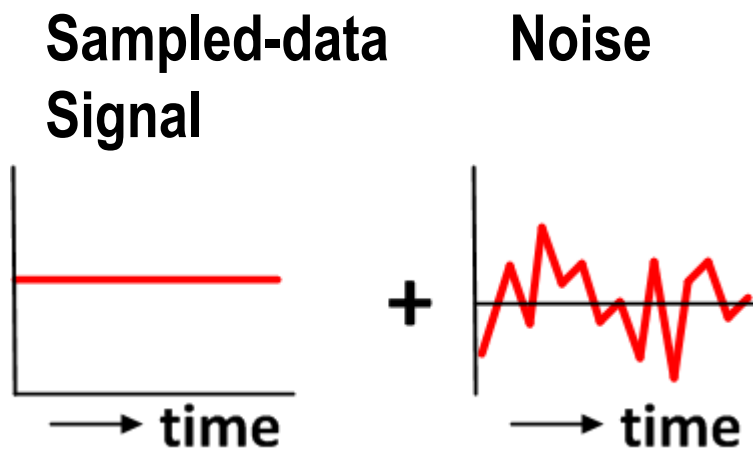
- **ADC Architecture**
- **Noise Filtering using Integrators**

Large Signals



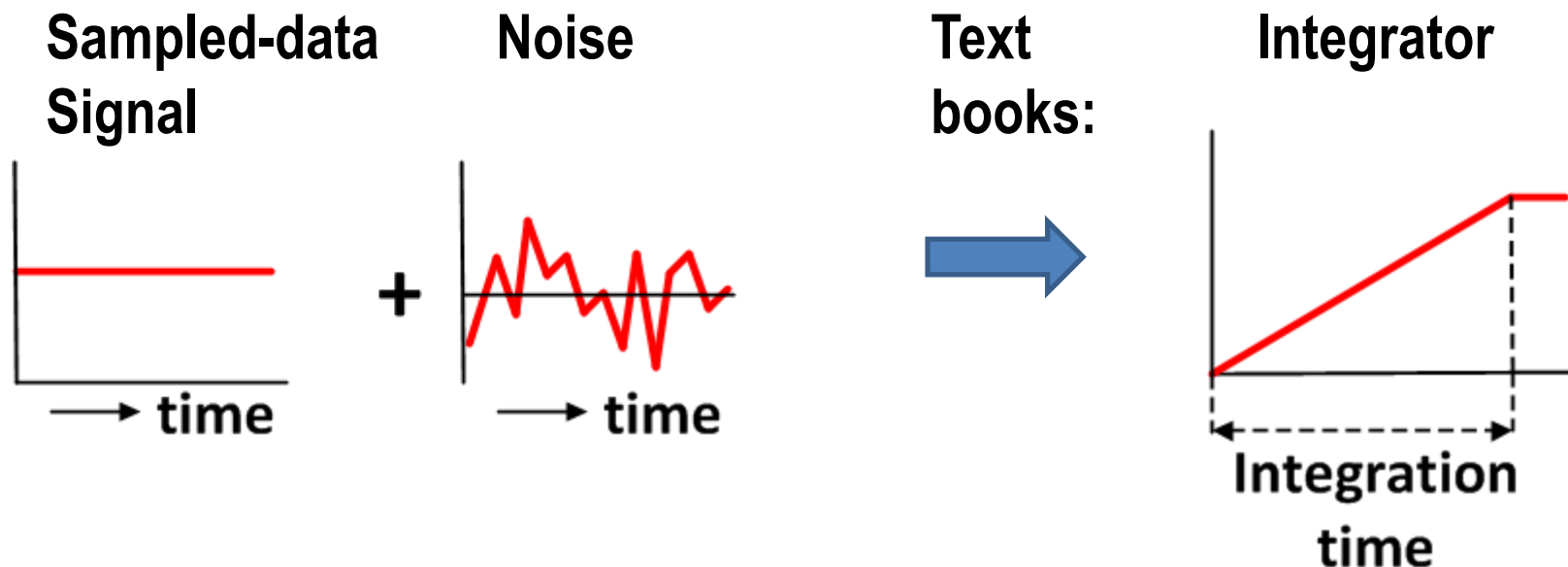
- **Reference Settling**
- **Reduced DAC Switching Energy**

Noise Filtering Principle



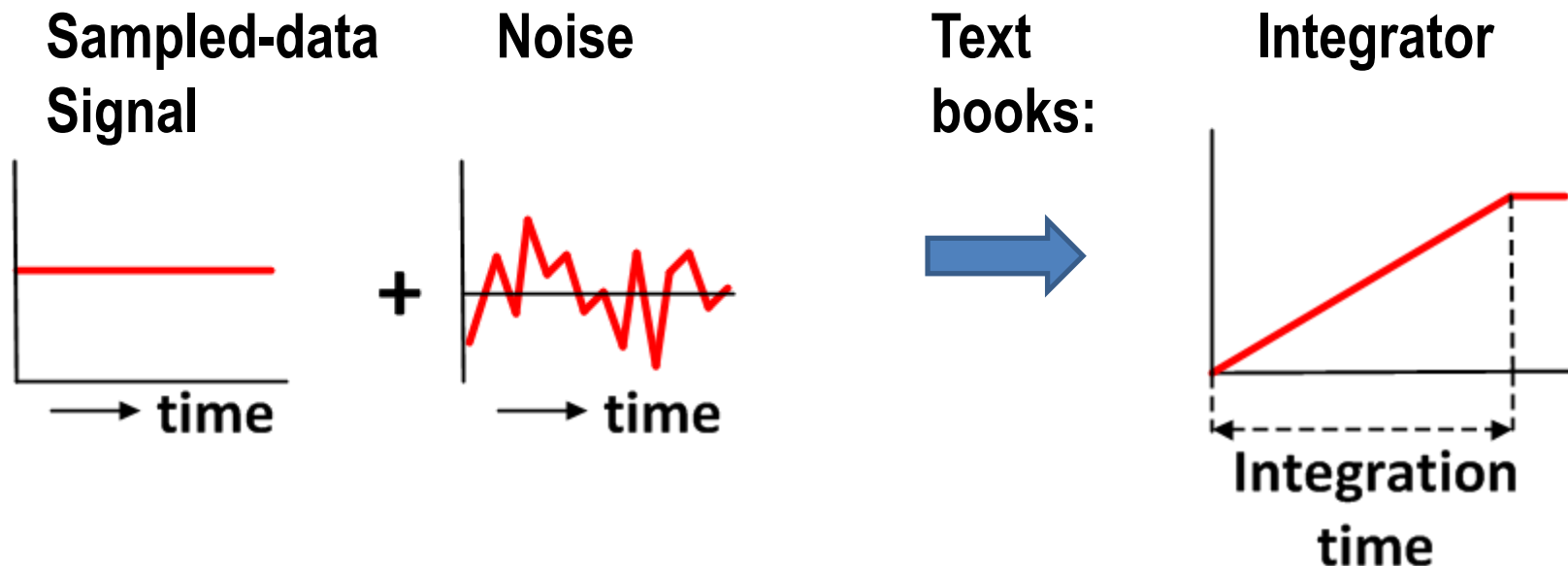
- Isolate sampled-data signal from noise

Noise Filtering Principle



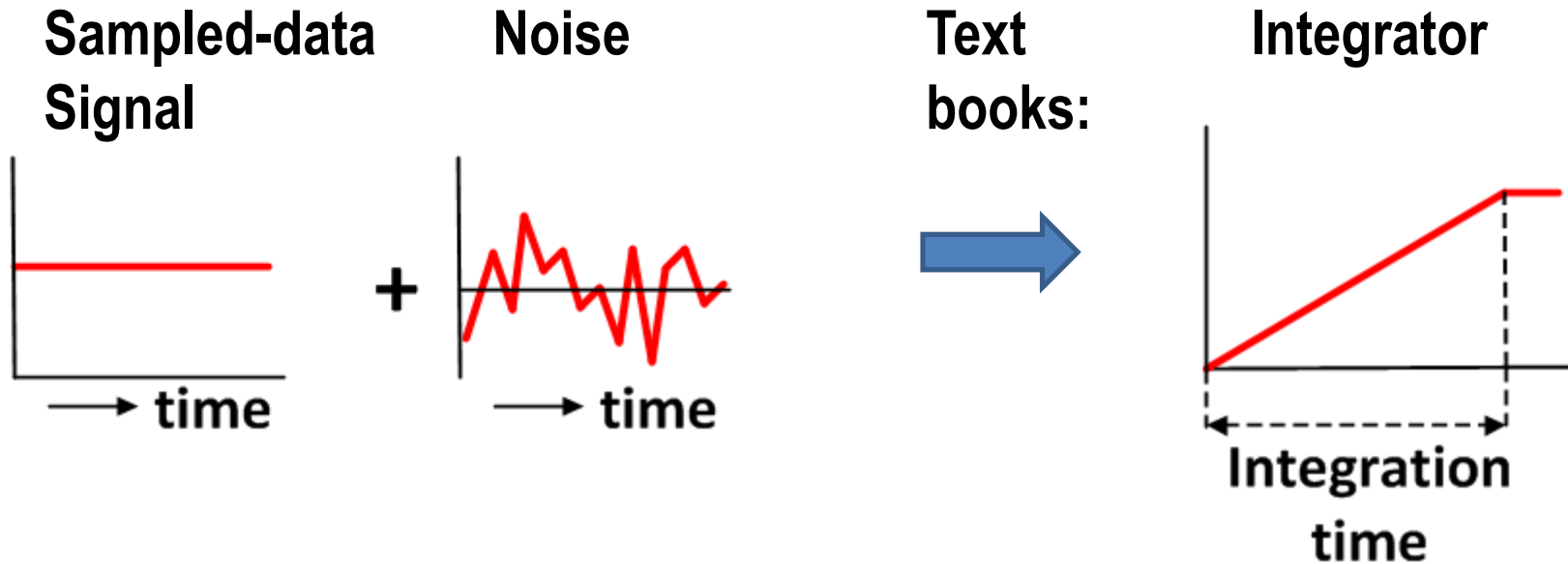
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Noise Filtering Principle



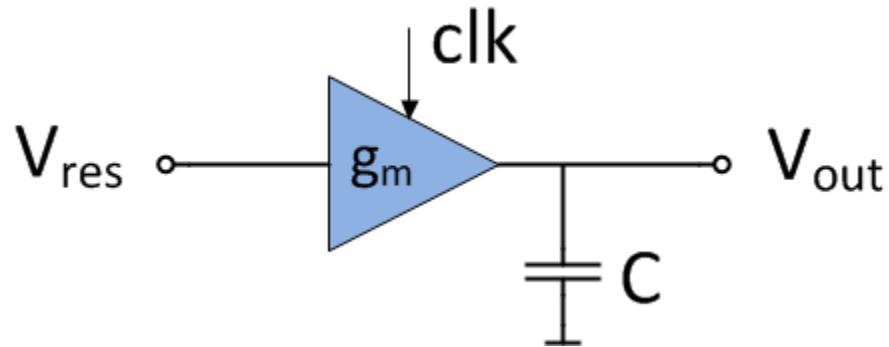
- Isolate sampled-data signal from noise
- Integrator: best SNR for a given time

Noise Filtering Principle

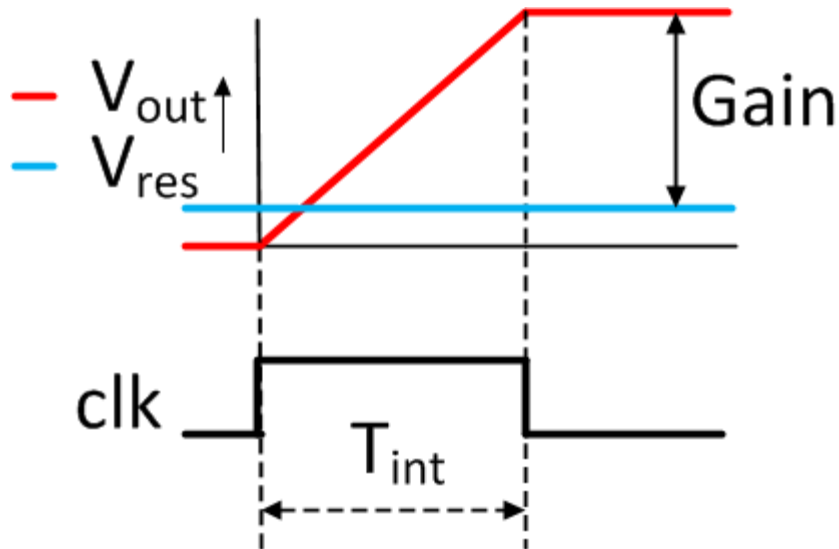
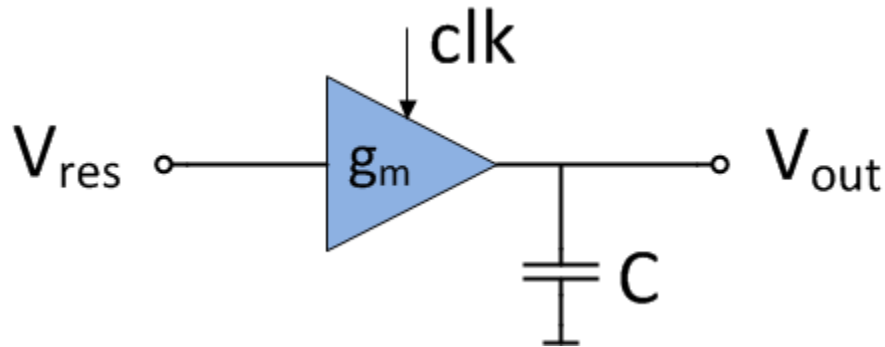


- Isolate sampled-data signal from noise
- Integrator: best SNR for a given time
- Apply integrator transfer to residue amplifier

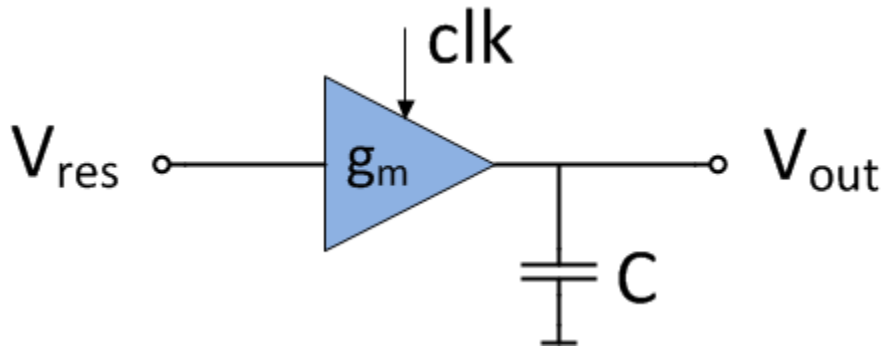
Making Gain with an Integrator



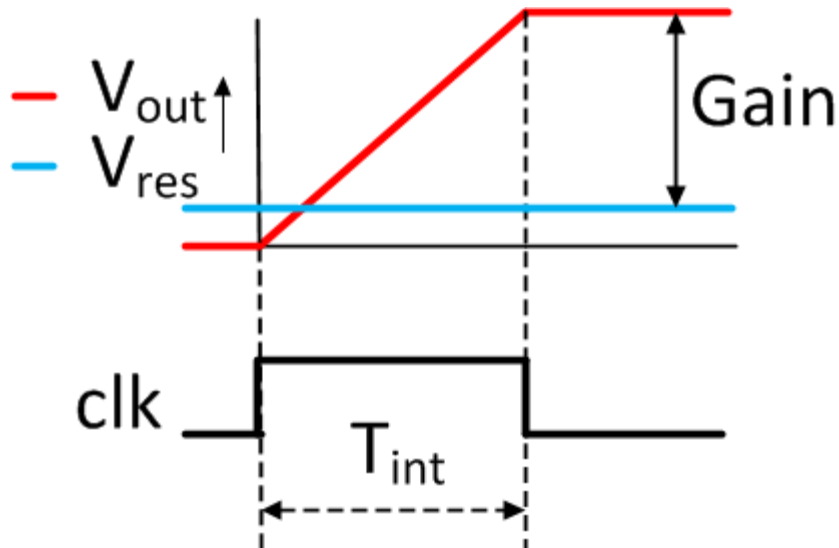
Making Gain with an Integrator



Making Gain with an Integrator

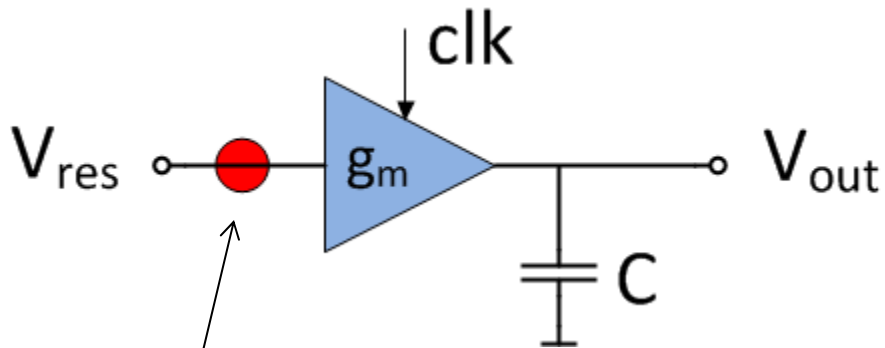


$$\text{Gain: } A = \left(\frac{g_m}{C} \right) T_{int}$$



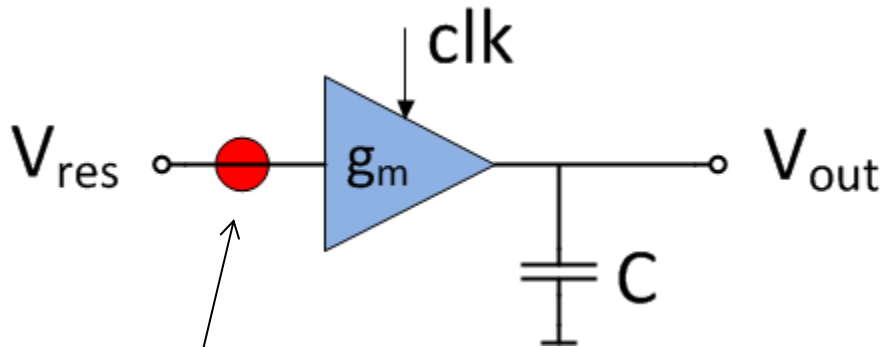
Gain proportional to T_{int}
 $\rightarrow T_{int}$ needs to be fixed

Some Math for Noise



$$\overline{u}_{n,dens} = \sqrt{4kT/g_m}$$

Some Math for Noise

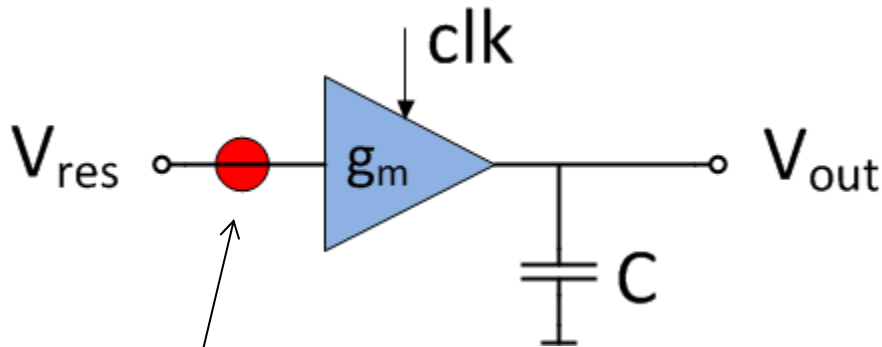


$$\overline{u}_{n,dens} = \sqrt{4kT/g_m}$$

Text books:

$$BW_{noise} = \frac{1}{2T_{int}}$$

Some Math for Noise



$$\bar{u}_{n,dens} = \sqrt{4kT/g_m}$$

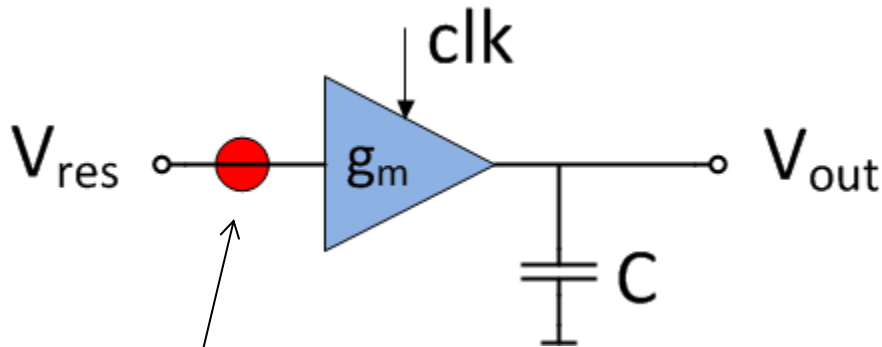
Text books:

$$BW_{noise} = \frac{1}{2T_{int}}$$

$$u_{n,i} = \sqrt{\frac{kT}{\frac{1}{2}AC}}$$

$u_{n,i} \rightarrow$ input referred noise
after integration time

Some Math for Noise



$$\bar{u}_{n,dens} = \sqrt{4kT/g_m}$$

Text books:

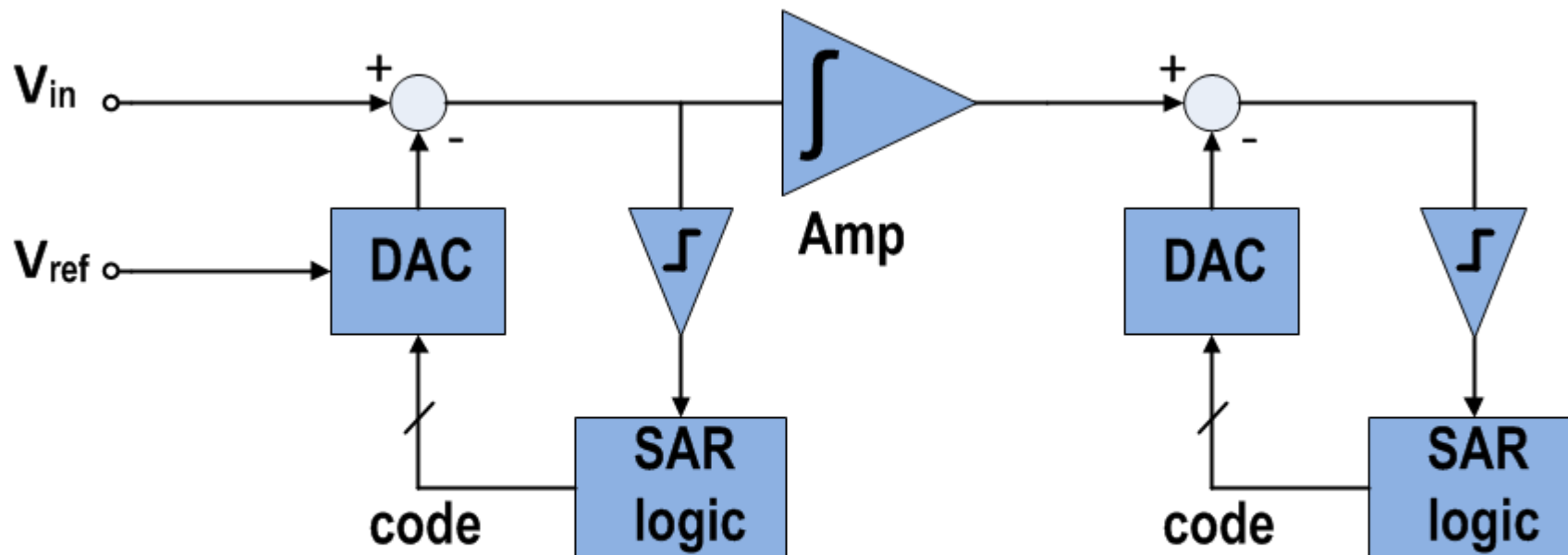
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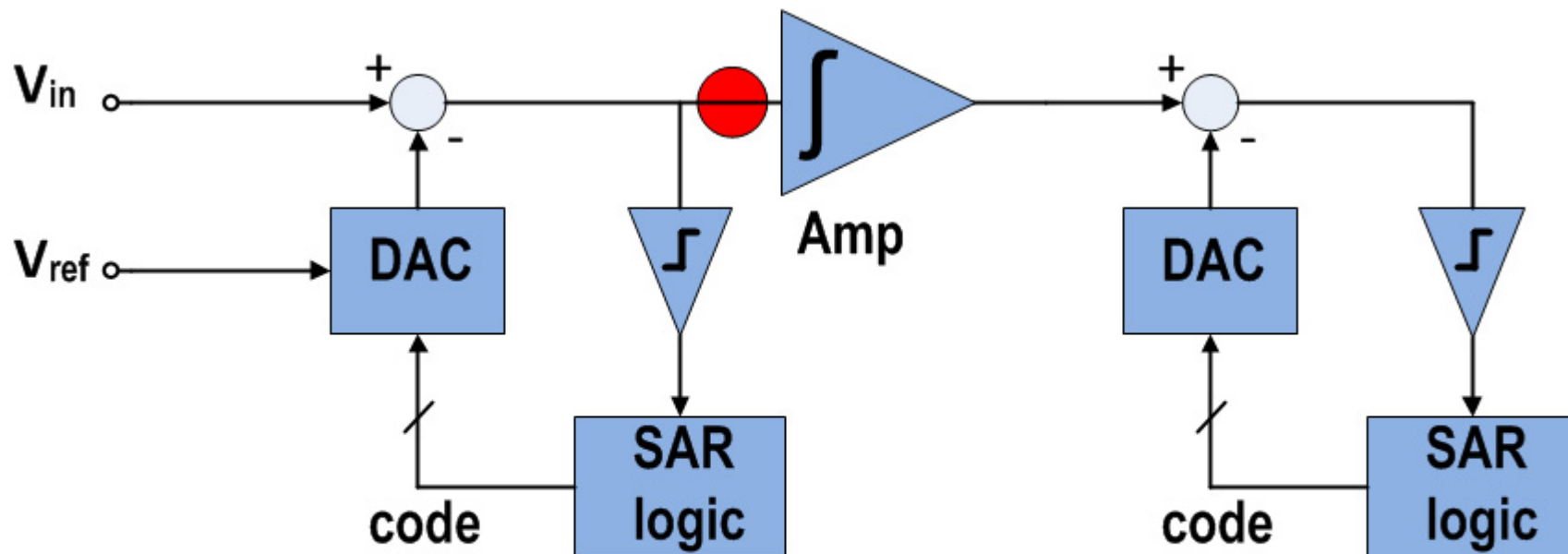
Low noise requires high gain and large caps

Major Noise Sources (excl. kT/C_s)



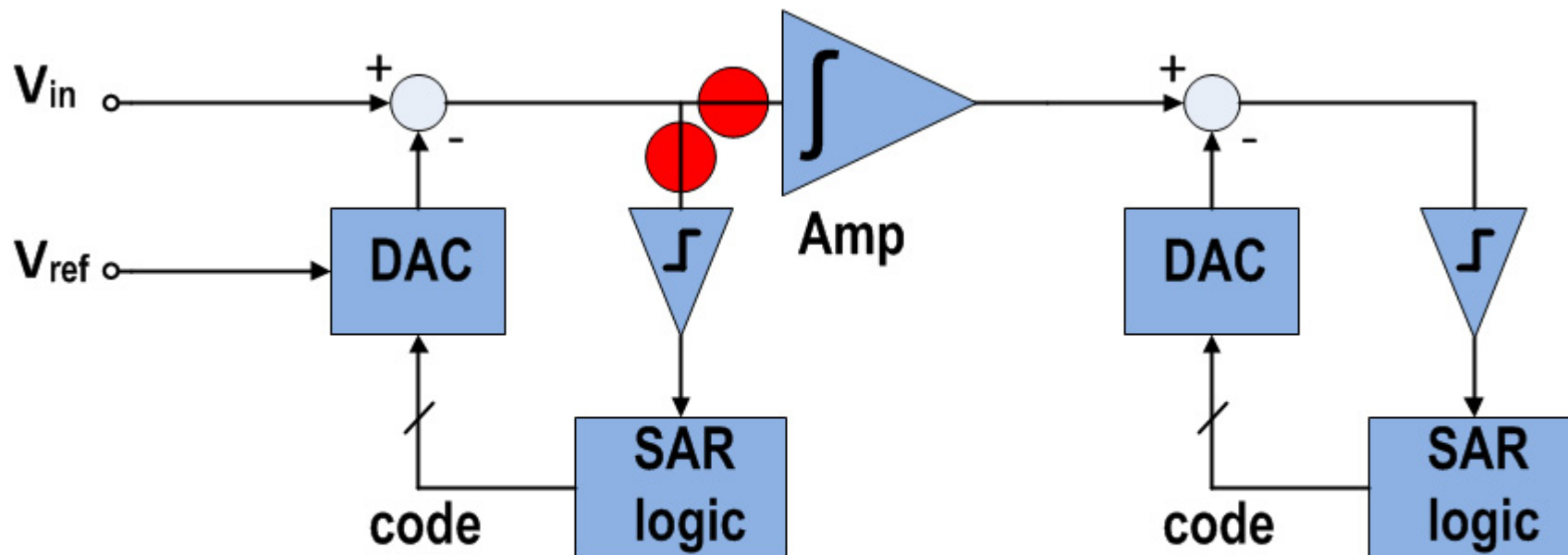
Noise Source	Solution

Major Noise Sources (excl. kT/C_s)



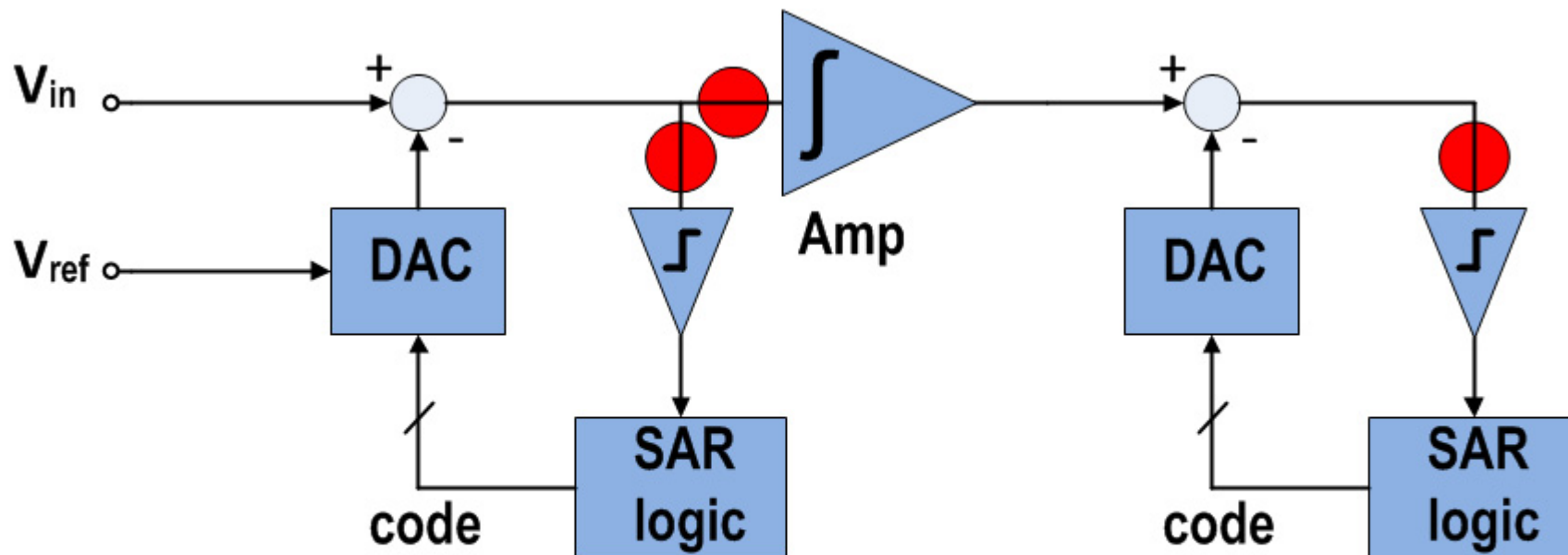
Noise Source	Solution
Residue Amplifier	Integrator

Major Noise Sources (excl. kT/C_s)



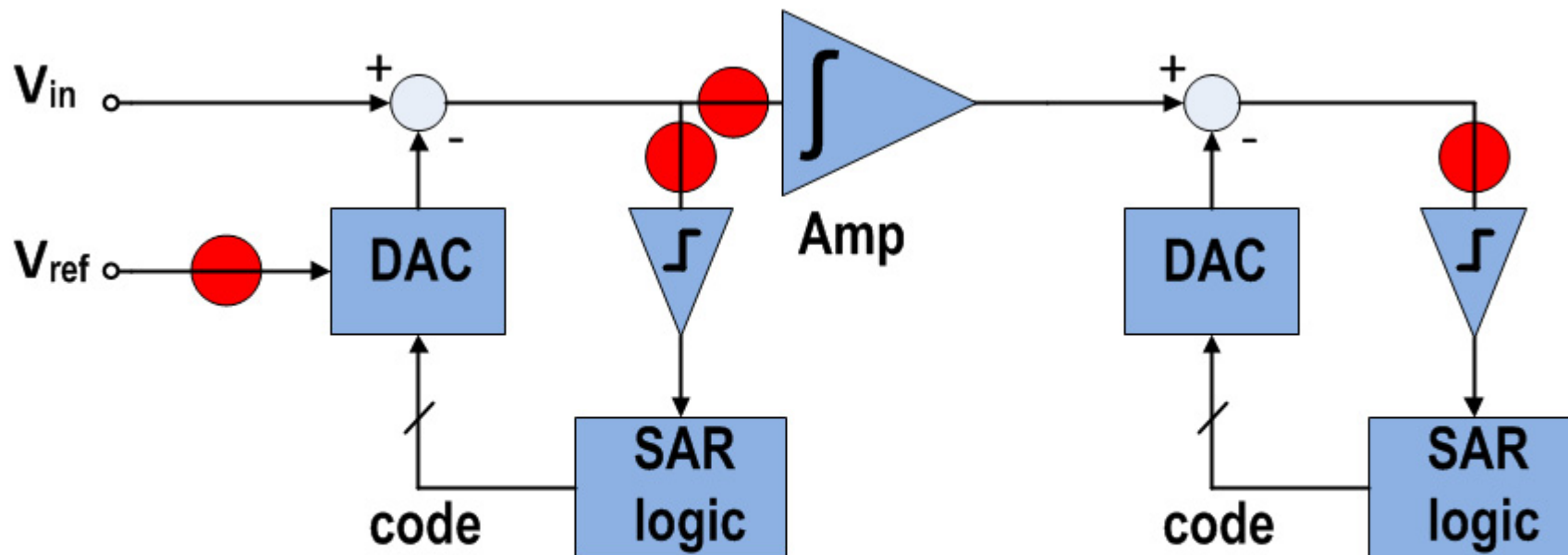
Noise Source	Solution
Residue Amplifier	Integrator
Stage-1 Comparator	Overrange between stages

Major Noise Sources (excl. kT/C_s)



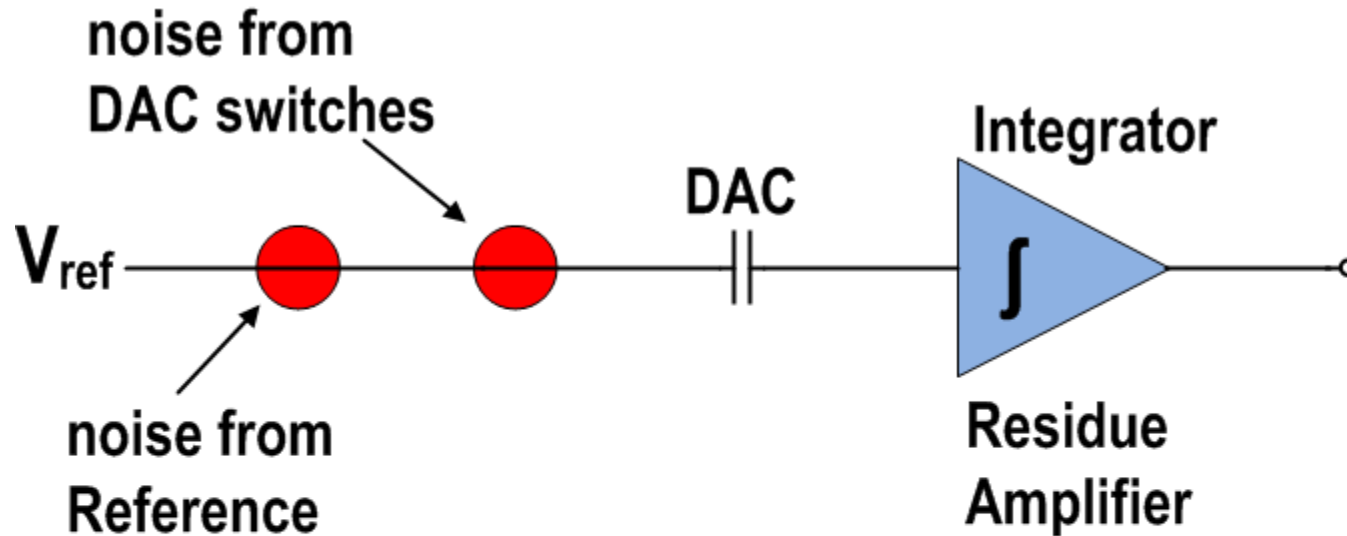
Noise Source	Solution
Residue Amplifier	Integrator
Stage-1 Comparator	Overrange between stages
Stage-2 Comparator	Gain of Residue Amplifier

Major Noise Sources (excl. kT/C_s)

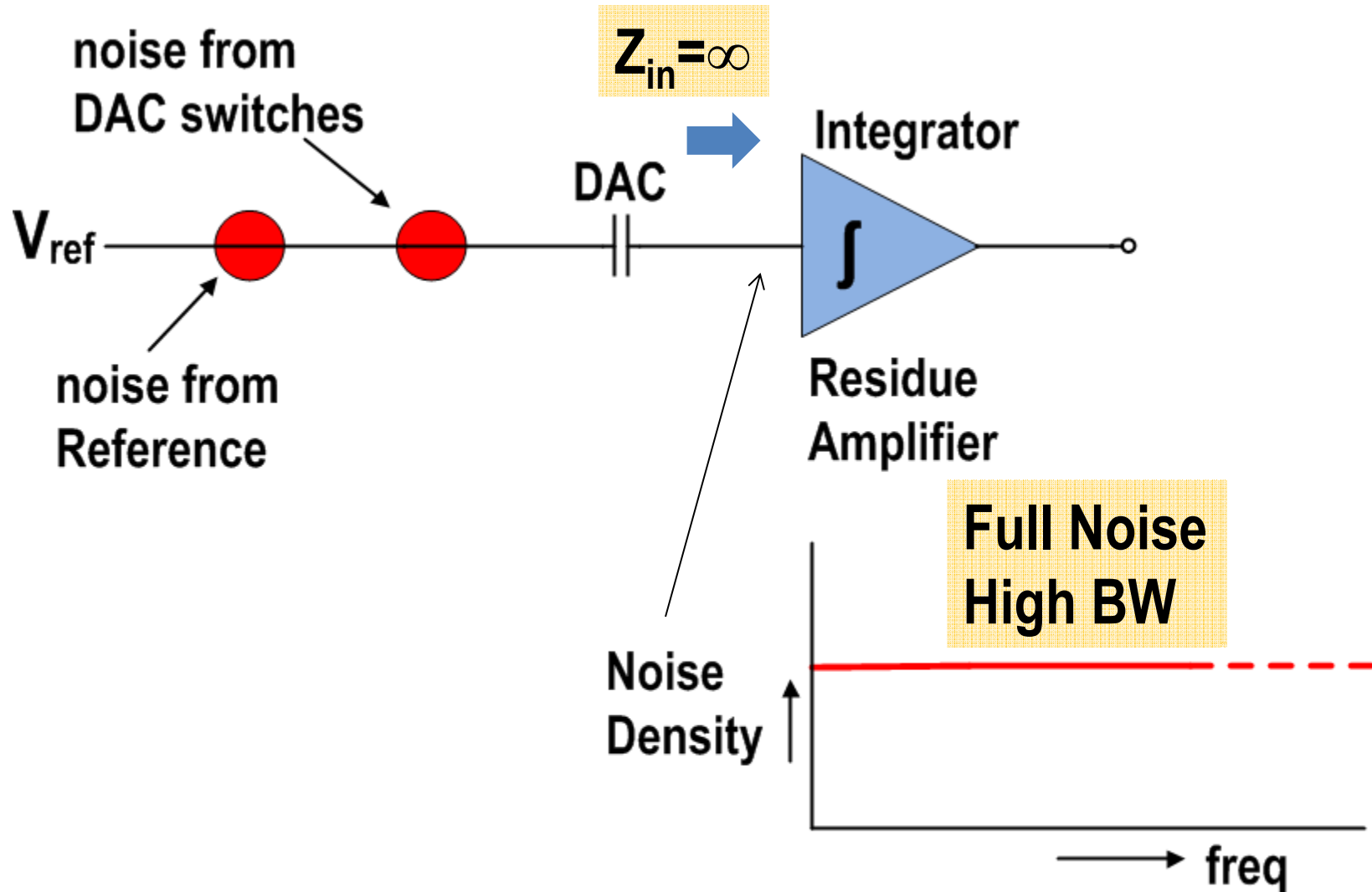


Noise Source	Solution
Residue Amplifier	Integrator
Stage-1 Comparator	Overrange between stages
Stage-2 Comparator	Gain of Residue Amplifier
Reference / DAC switches	Integrator

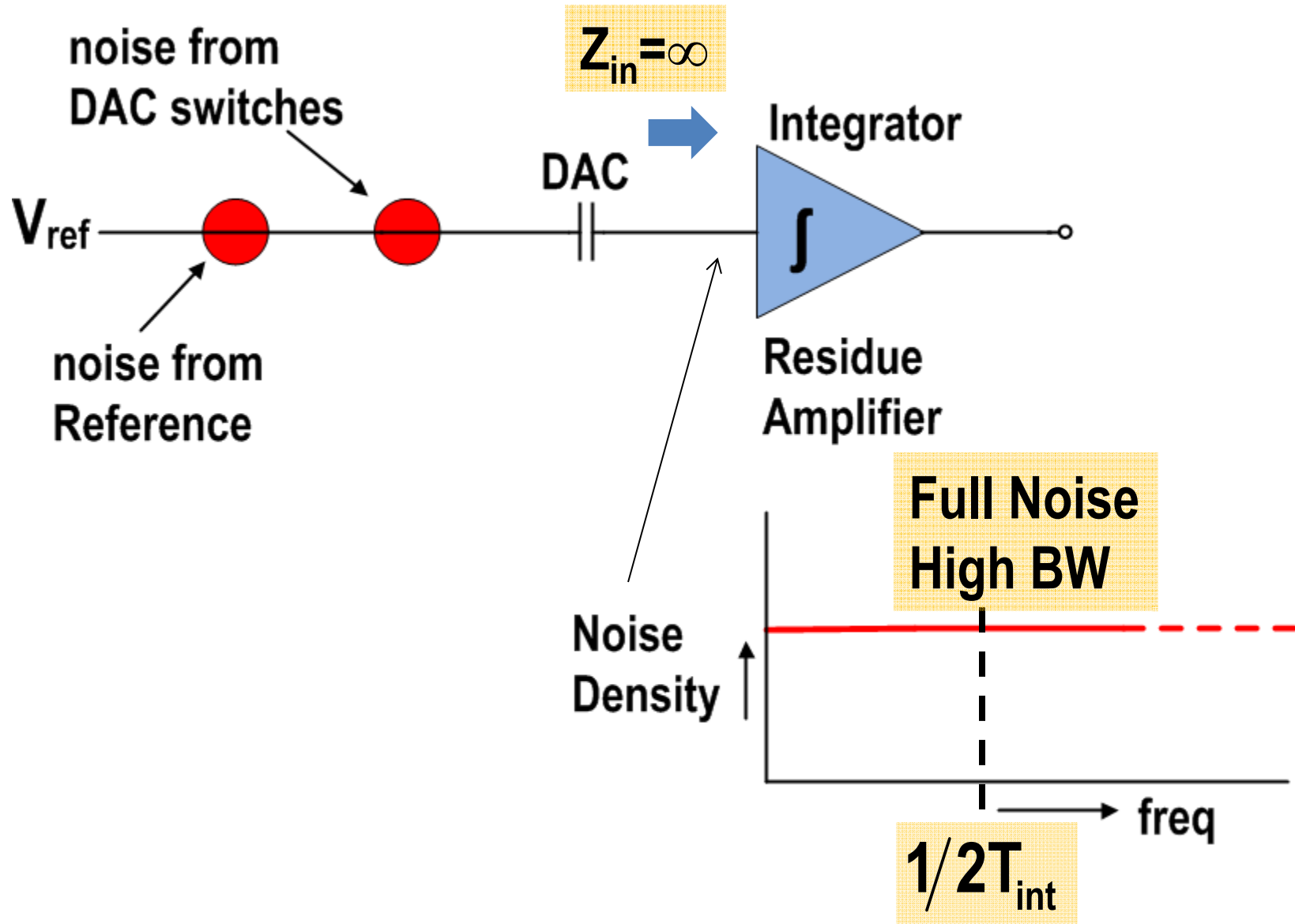
Full Reference Noise at +/- Full-Scale



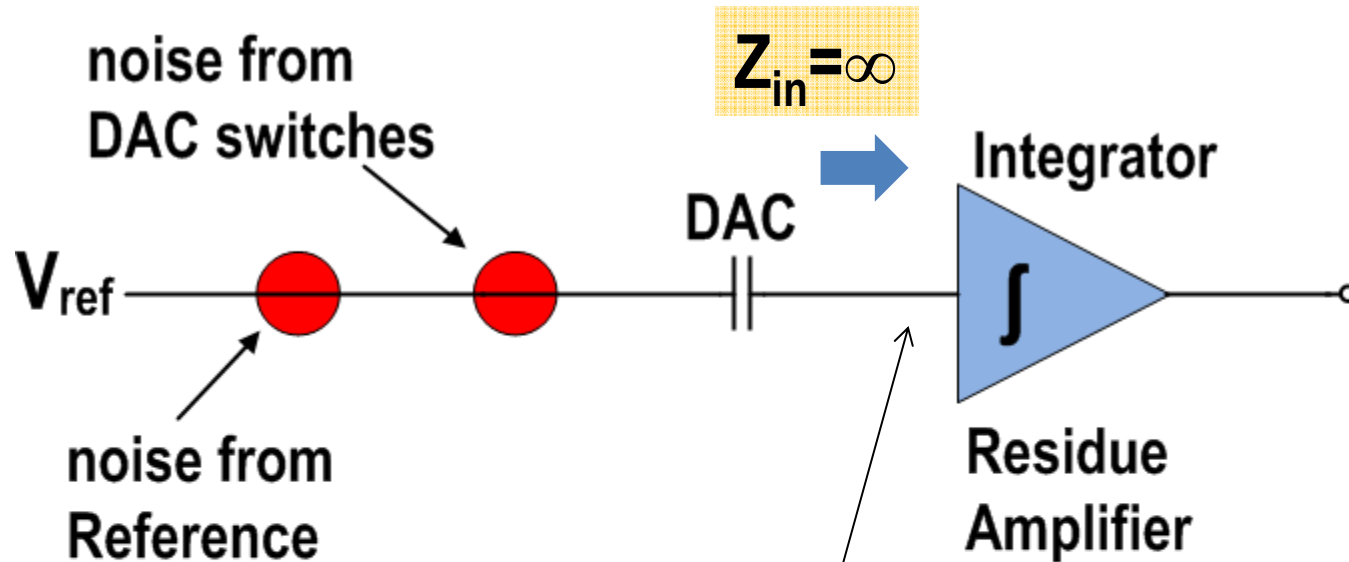
Full Reference Noise at +/- Full-Scale



Full Reference Noise at +/- Full-Scale

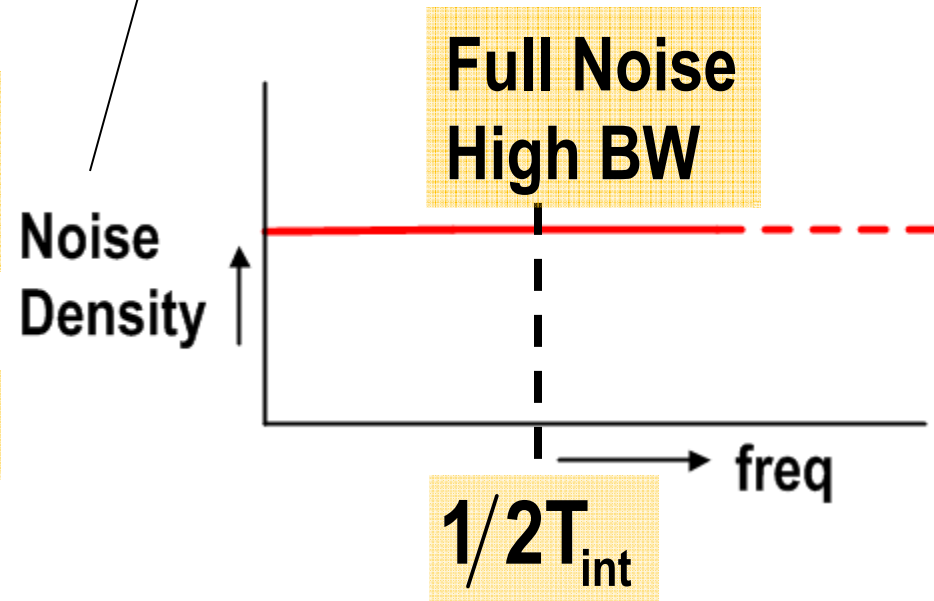


Full Reference Noise at +/- Full-Scale



Integrator: strongest filtering of noise at its input

Save power in Reference



Residue Amplifier specifications

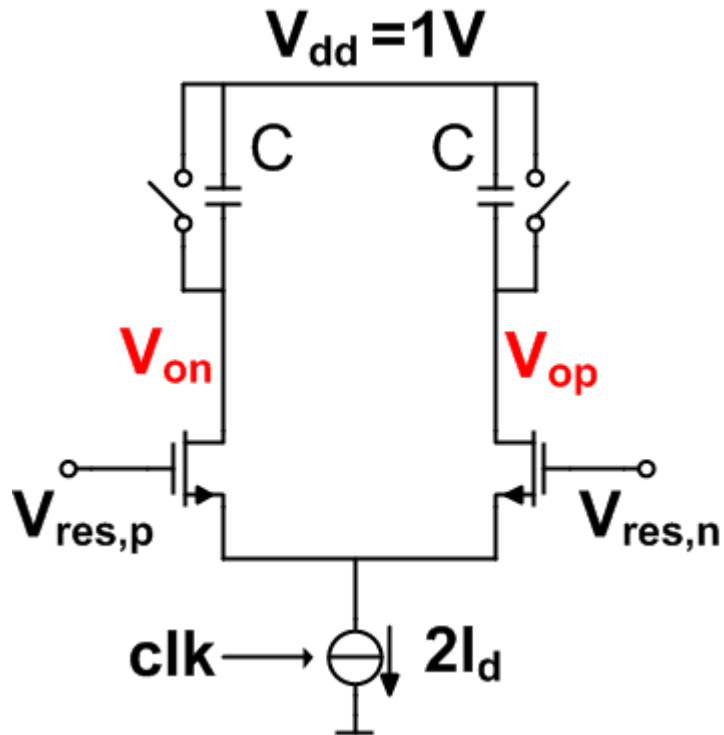
Required Gain: 16x

- **Allows using a low-power comparator in stage 2**

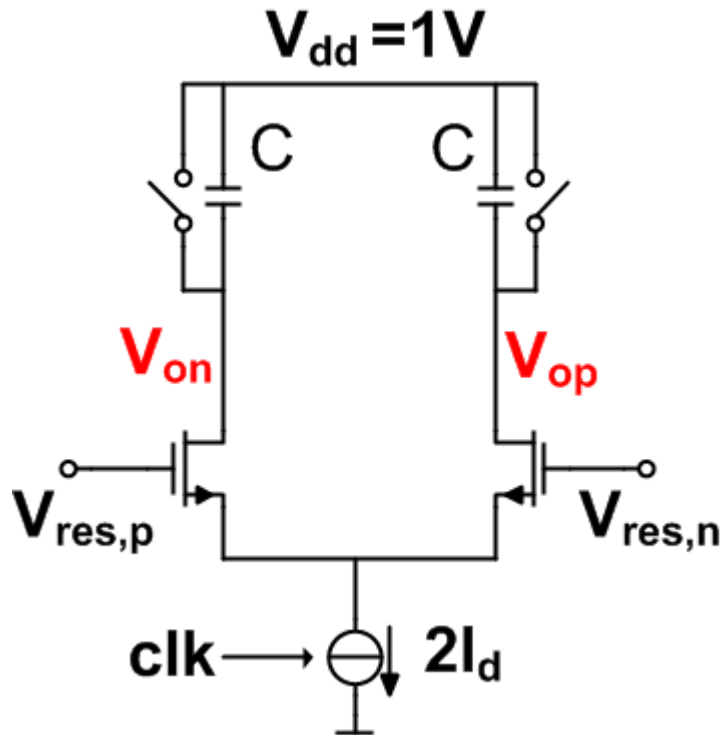
Ideal integrator transfer during available time

- **Best SNR (noise from residue amplifier)**
- **Best filtering of noise from Reference Generator and DAC switches**

Residue Amplifier: transistor implementation



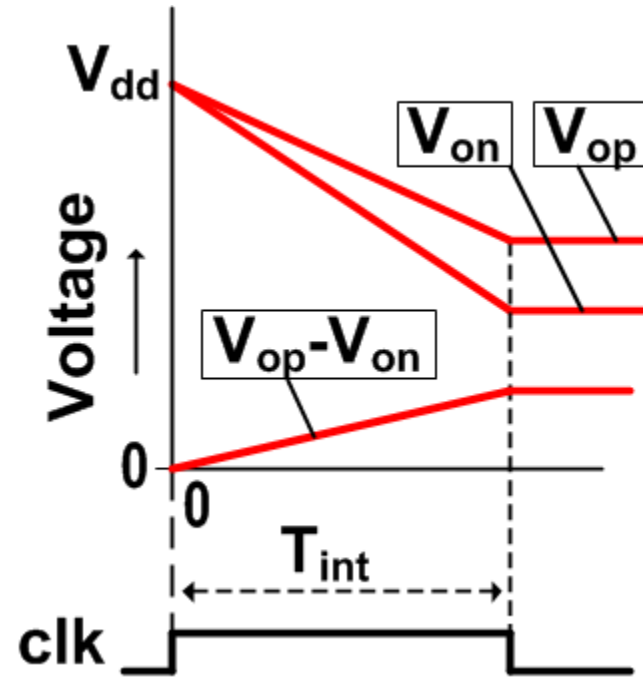
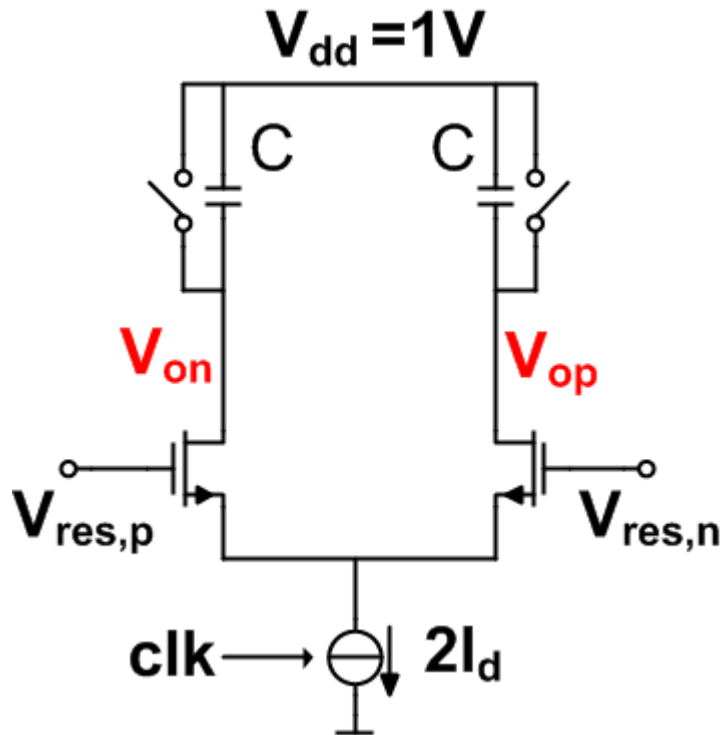
Residue Amplifier: transistor implementation



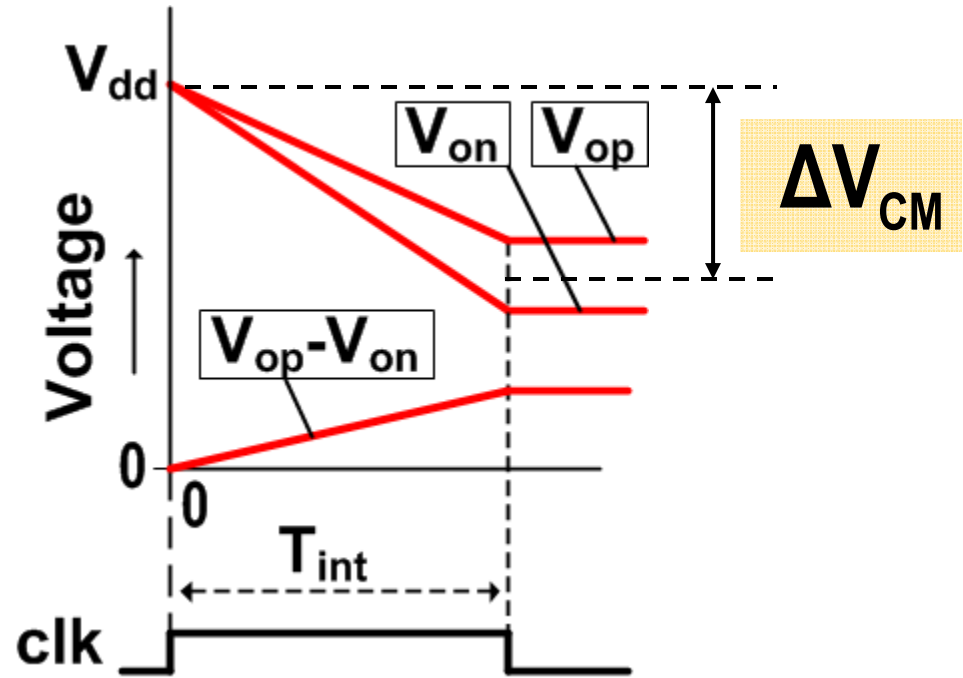
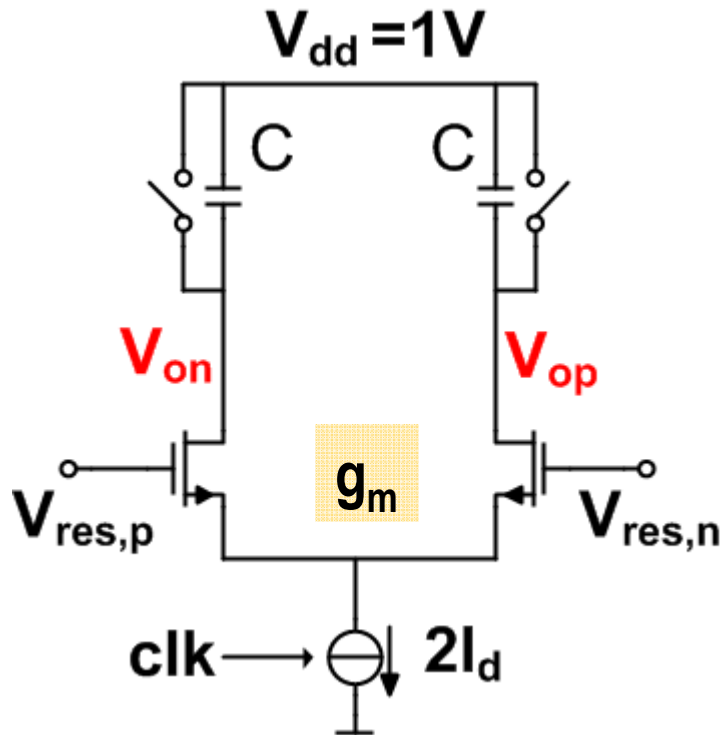
- Differential pair and capacitors
- Only input transistors generate noise
 - Ignore switches

- Dynamic operation (clocked)
- CM of output changes
 - bias current flows through load caps C

Residue Amplifier: transistor implementation

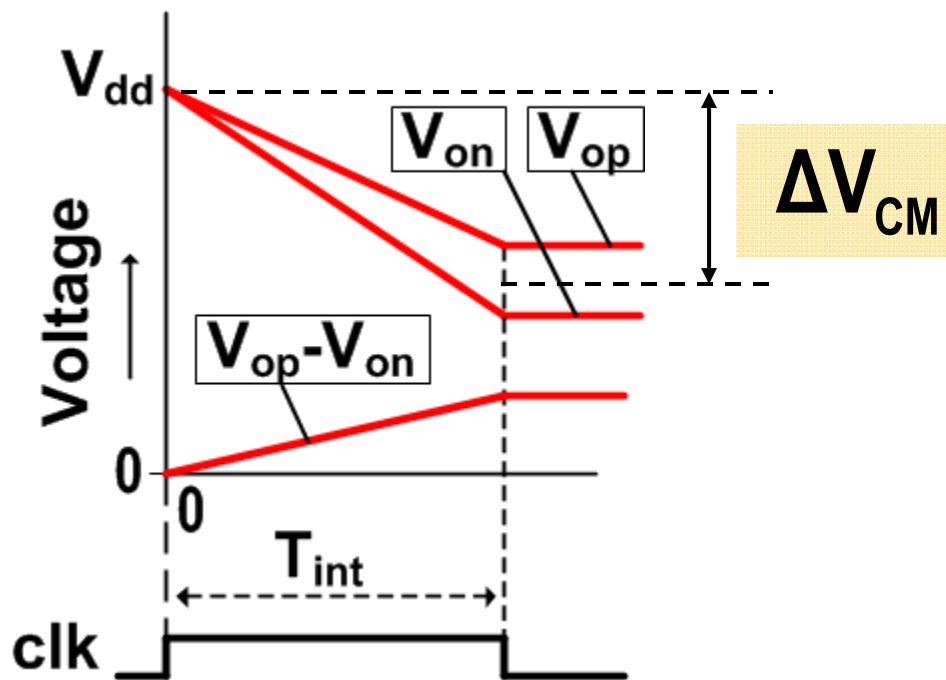
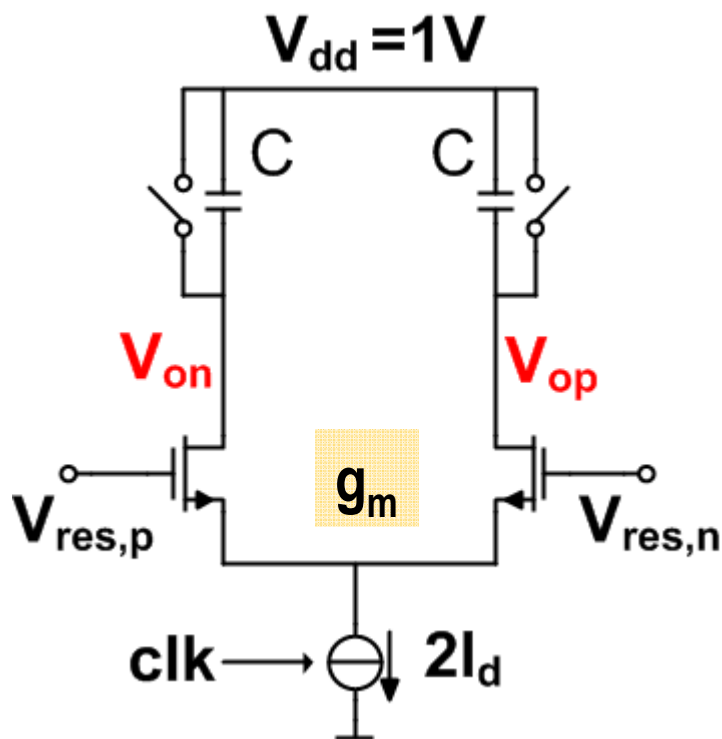


Residue Amplifier: transistor implementation



Gain proportional to g_m and ΔV_{cm}

Residue Amplifier: transistor implementation



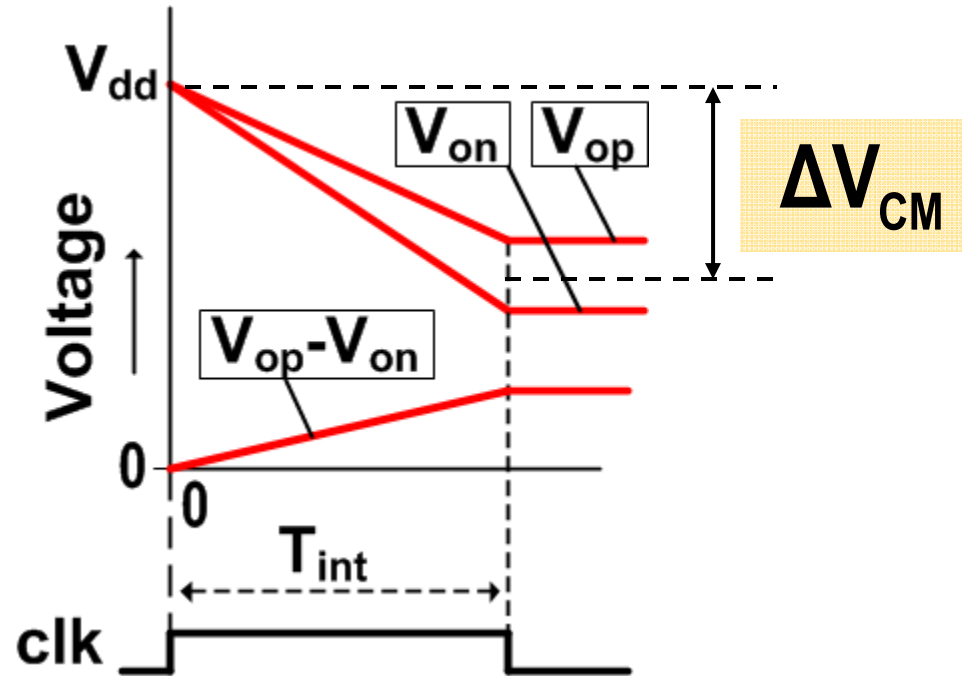
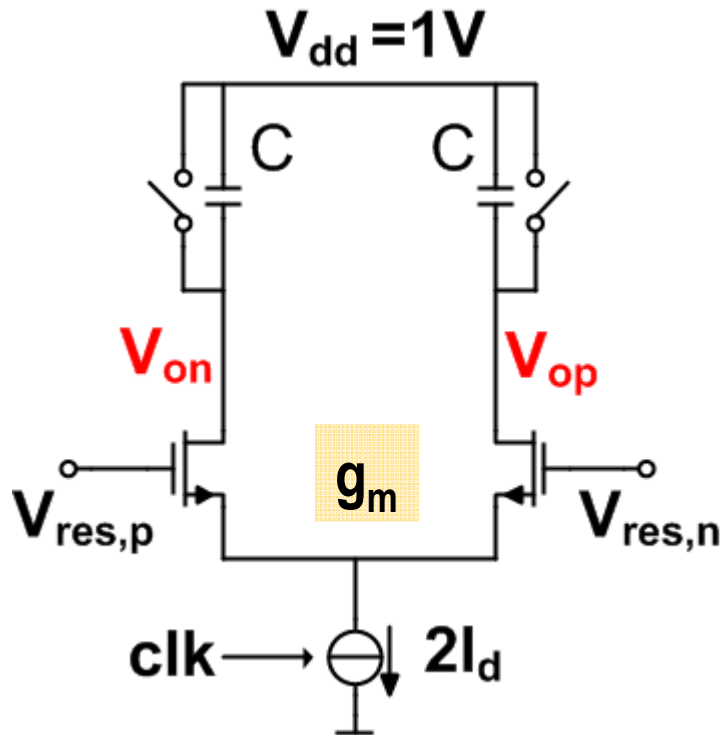
Gain proportional to g_m and ΔV_{cm}

Weak Inversion: $g_m / I_d = 1/50mV$

ΔV_{cm} limited to about 500mV

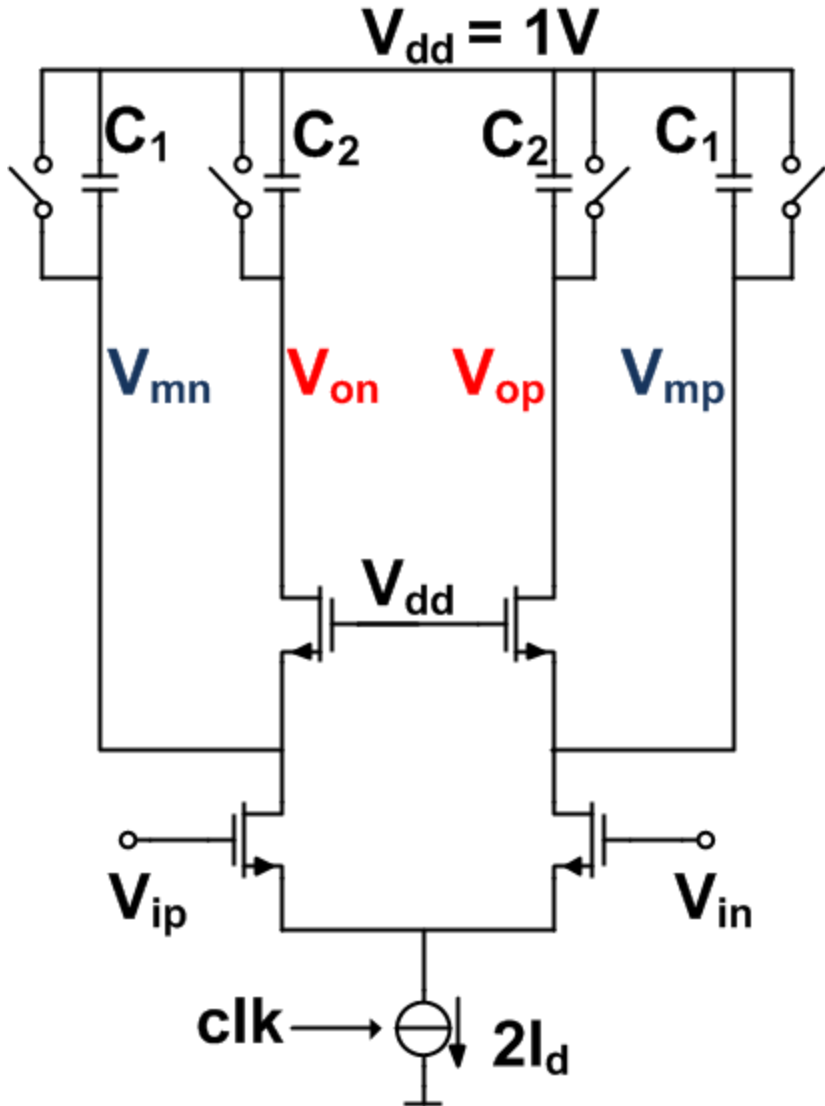
Gain = 10x

Increasing the Gain



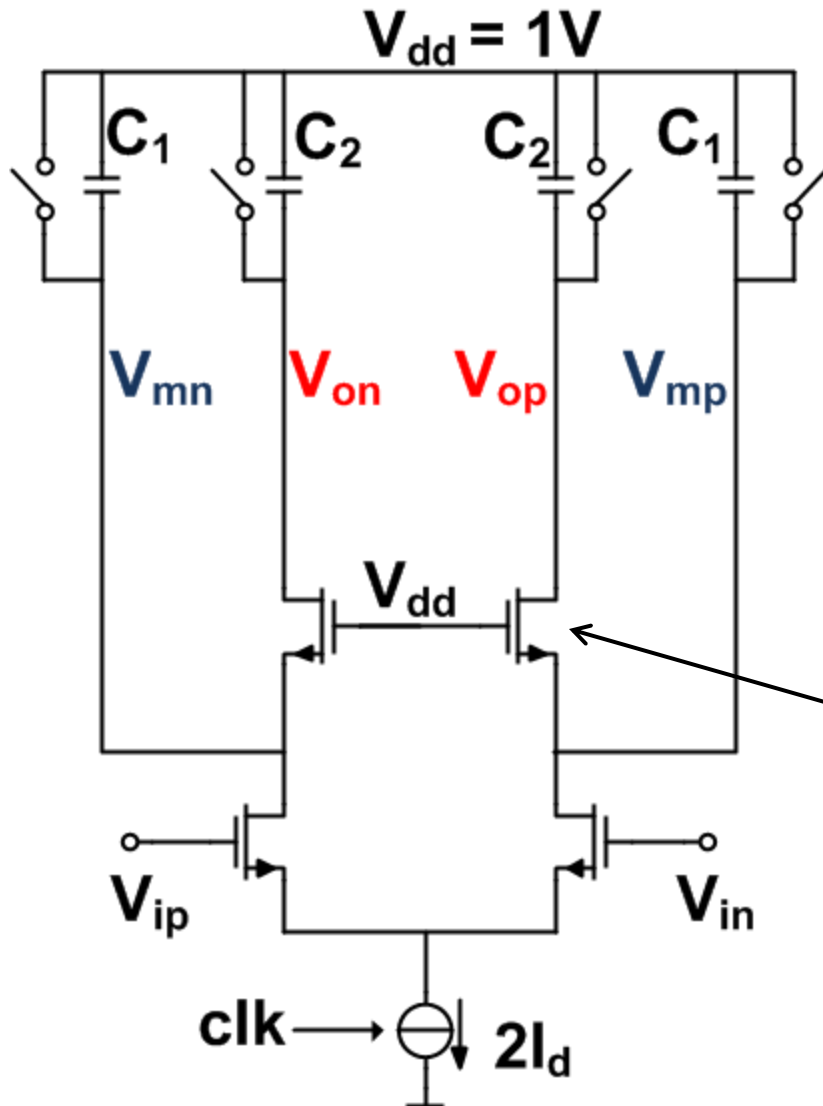
- Gain does not depend on C (C smaller $\rightarrow T_{int}$ shorter)
- g_m already at max.
- Need larger $\Delta V_{cm} \rightarrow$ higher supply voltage

Virtual boost of ΔV_{cm}



- **Virtual boost of ΔV_{cm}**
- **No high supply needed**
- **Gain increased**

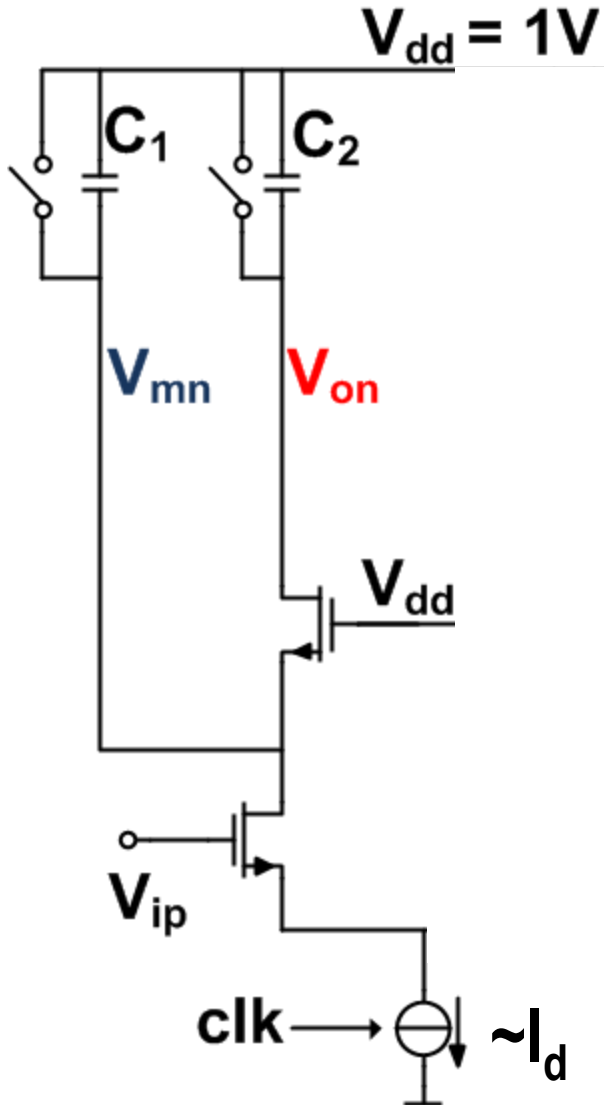
Virtual boost of ΔV_{cm}



- Virtual increase of ΔV_{cm}
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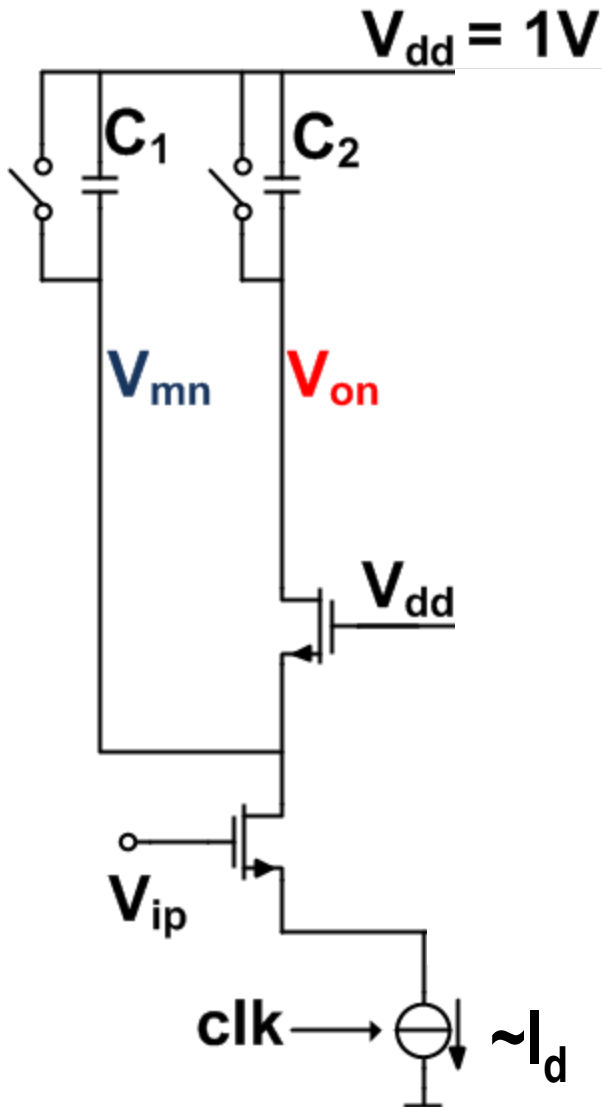
Cascodes turn on during integration

Operation principle (1/7)

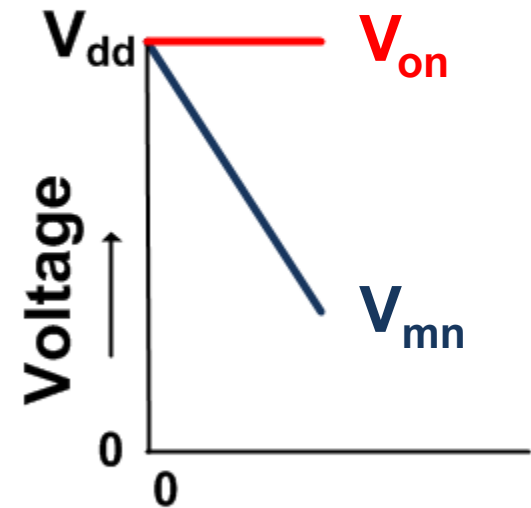


Branch current close to I_d

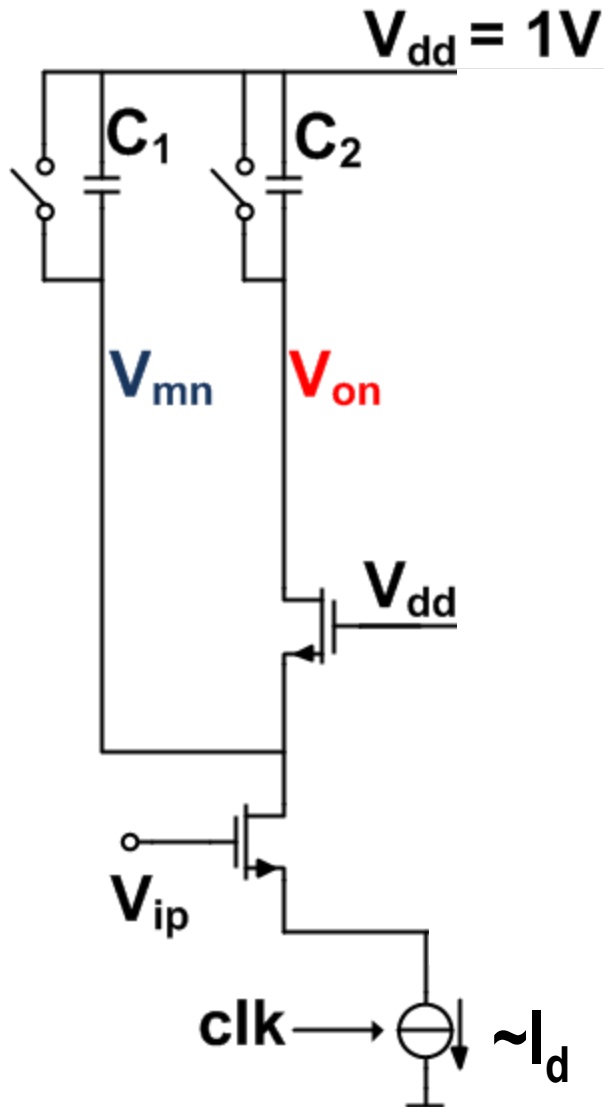
Operation principle (2/7)



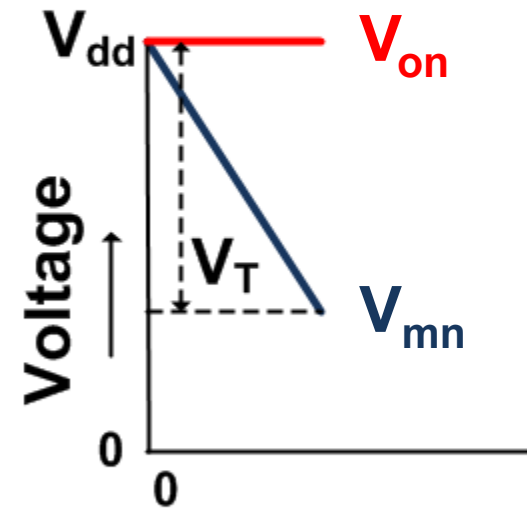
Integration on C_1



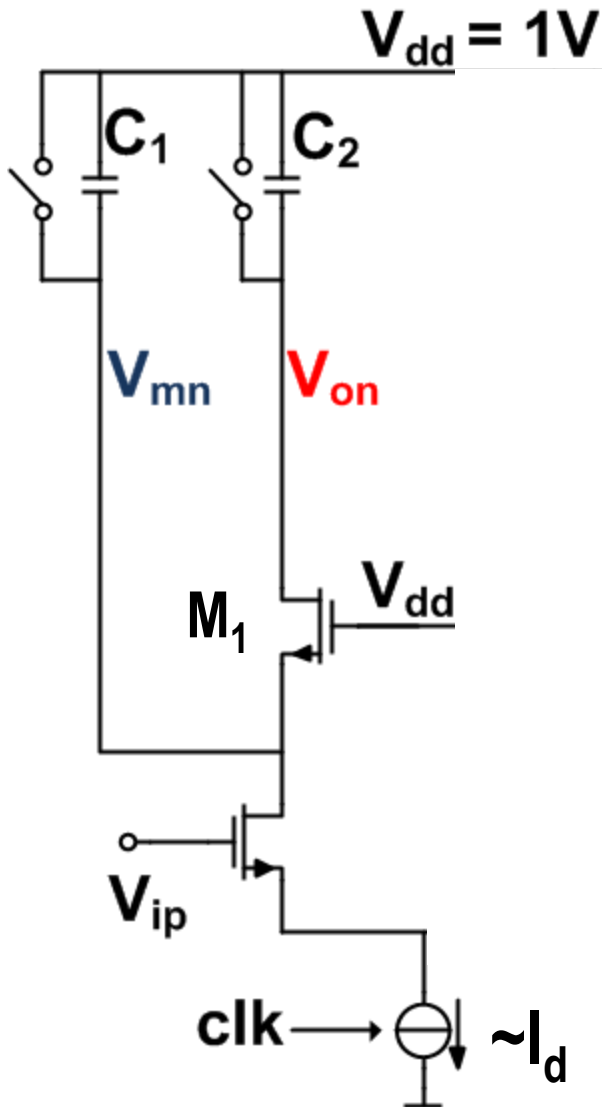
Operation principle (3/7)



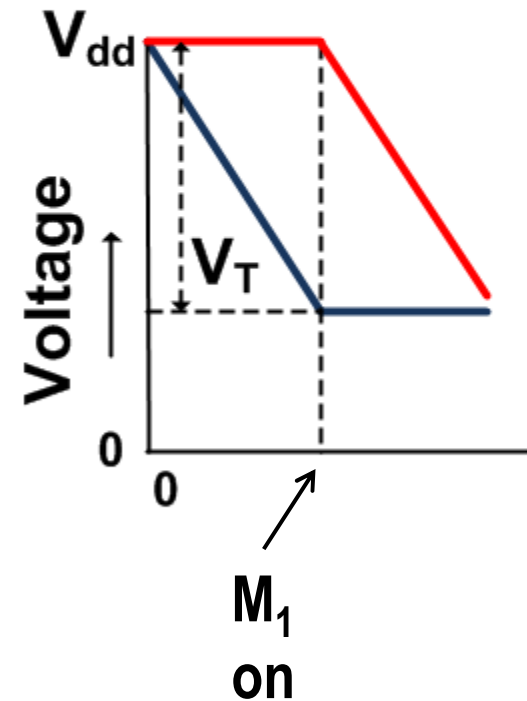
Integration on C_1



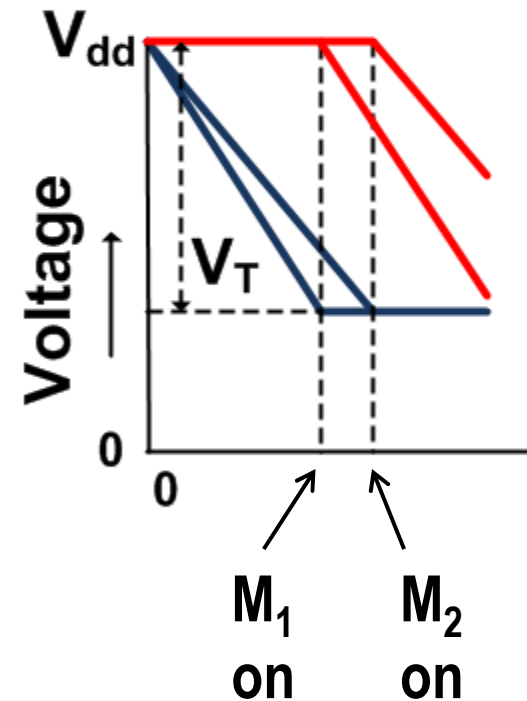
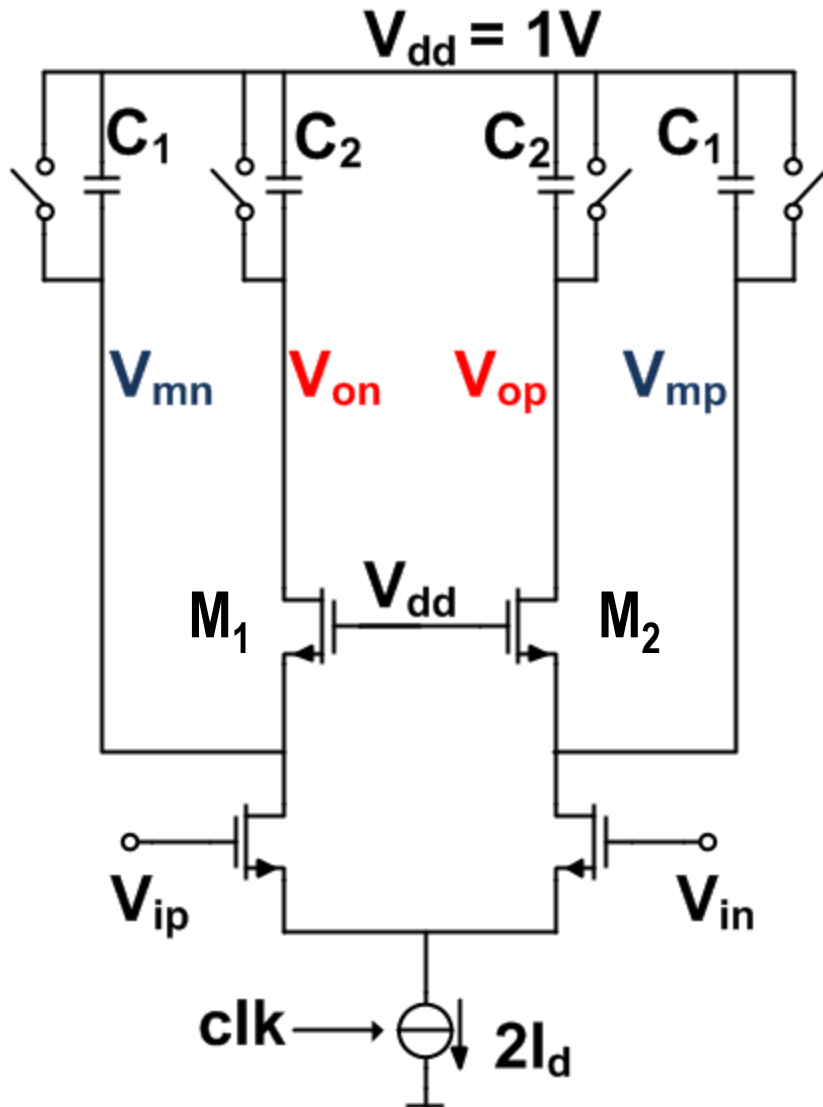
Operation principle (4/7)



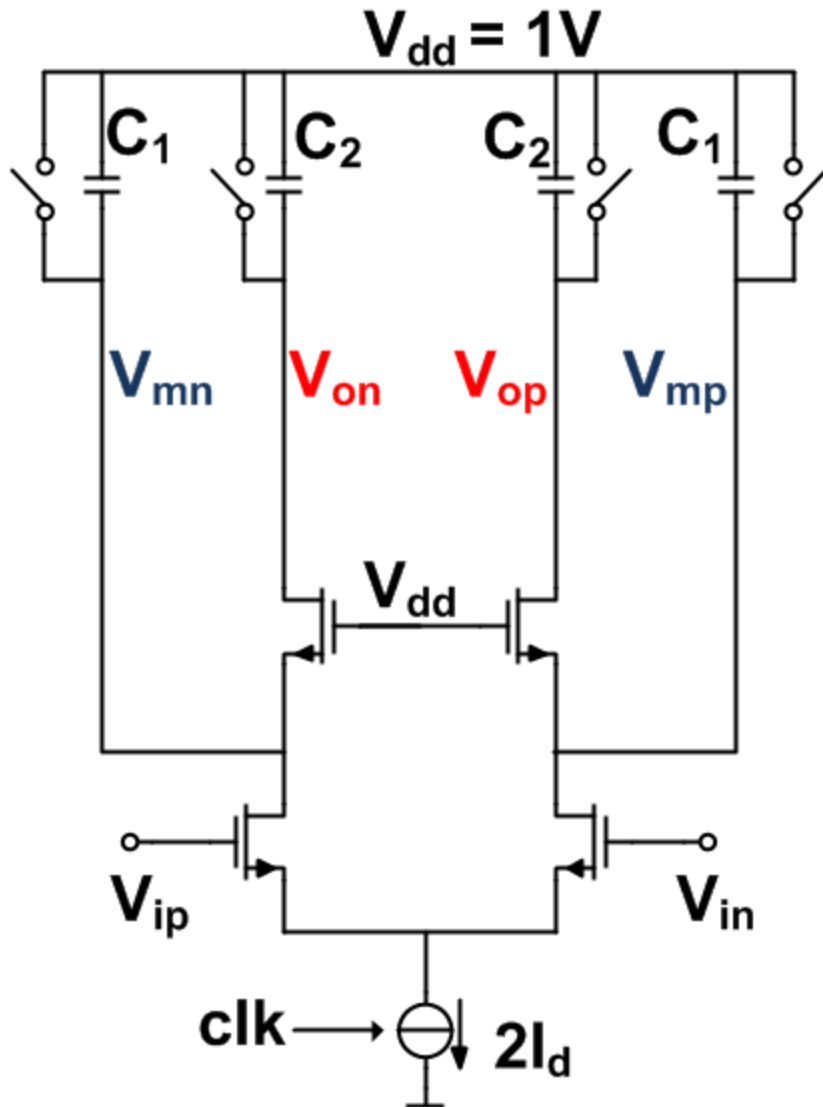
Integration on C_2



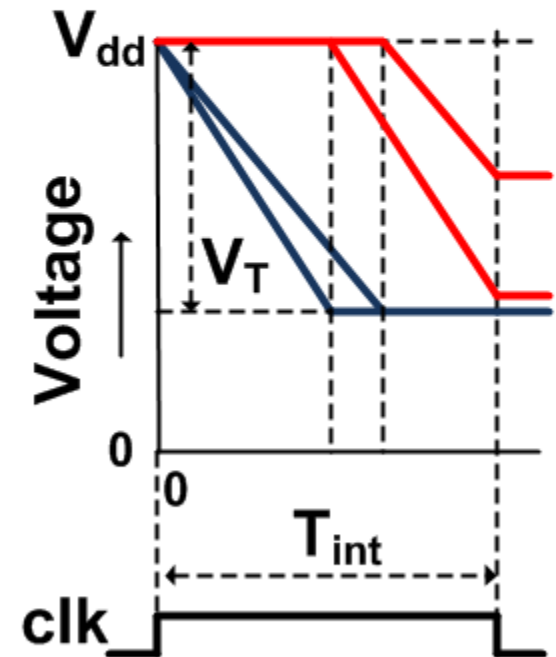
Operation principle (5/7)



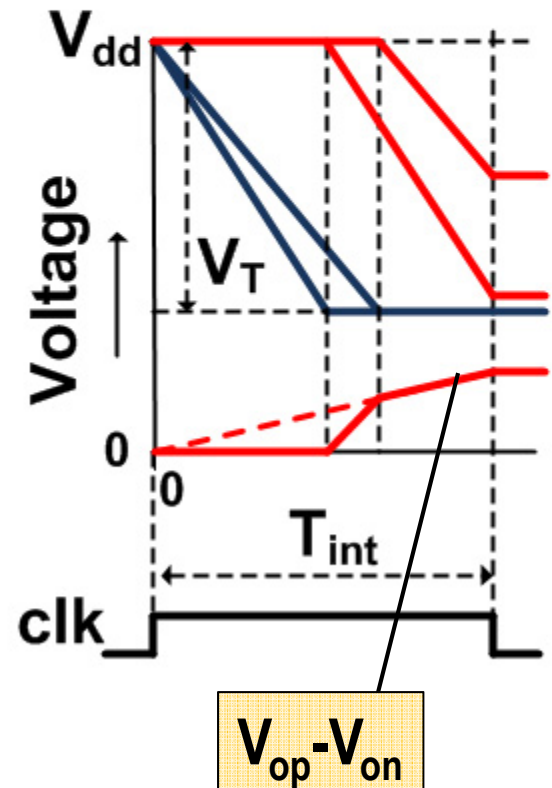
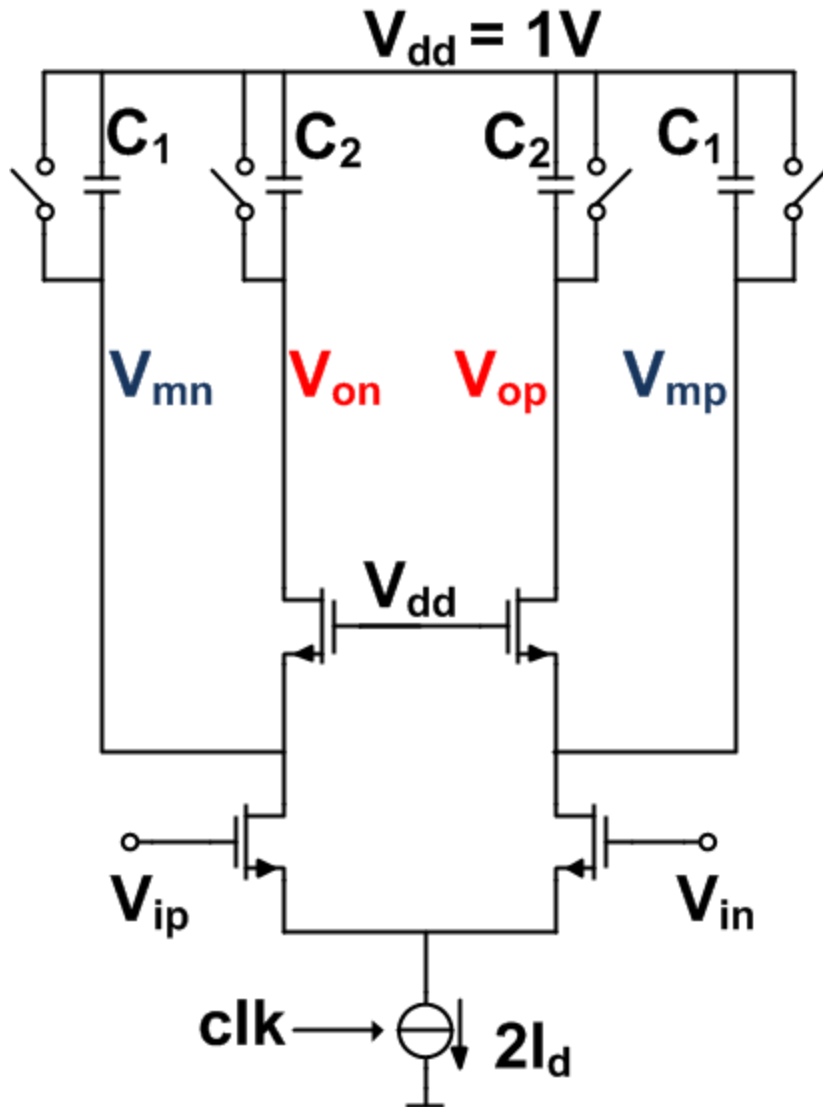
Operation principle (6/7)



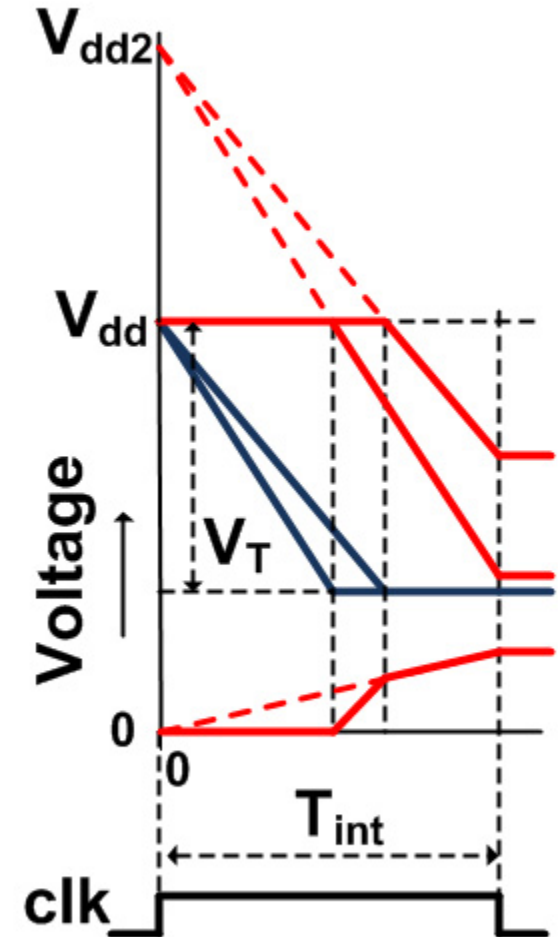
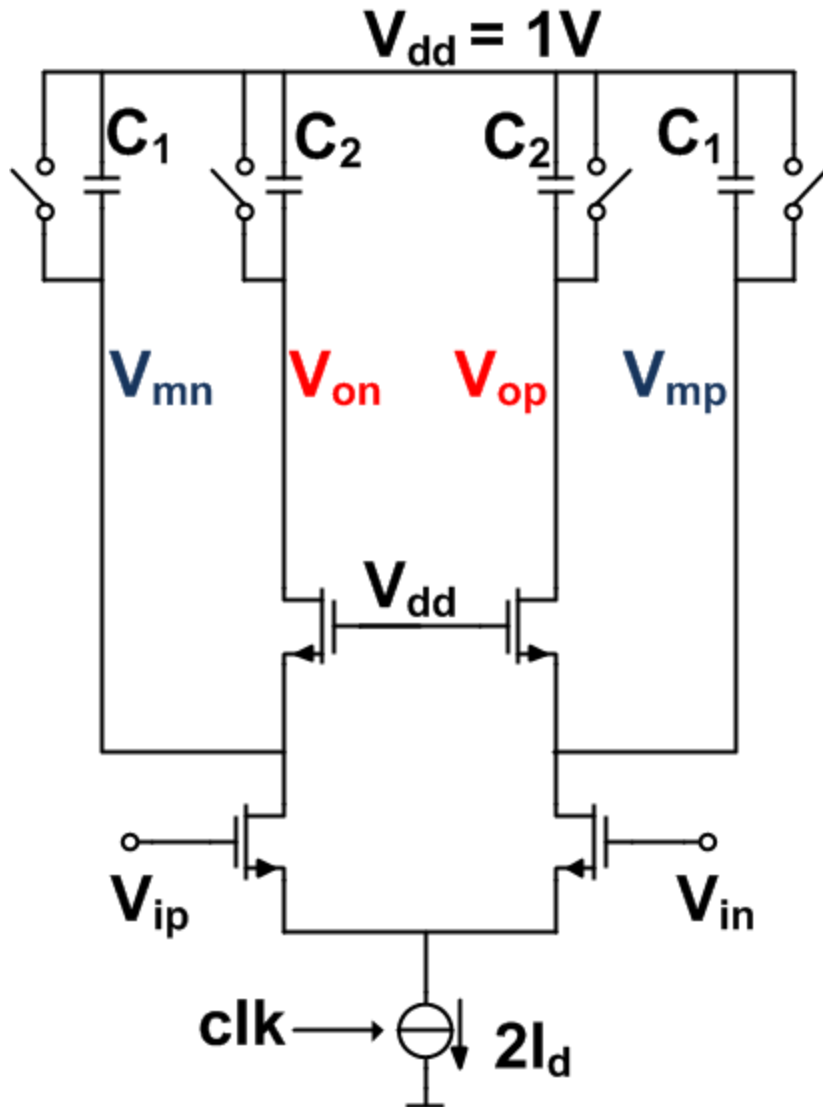
CLK stops integration



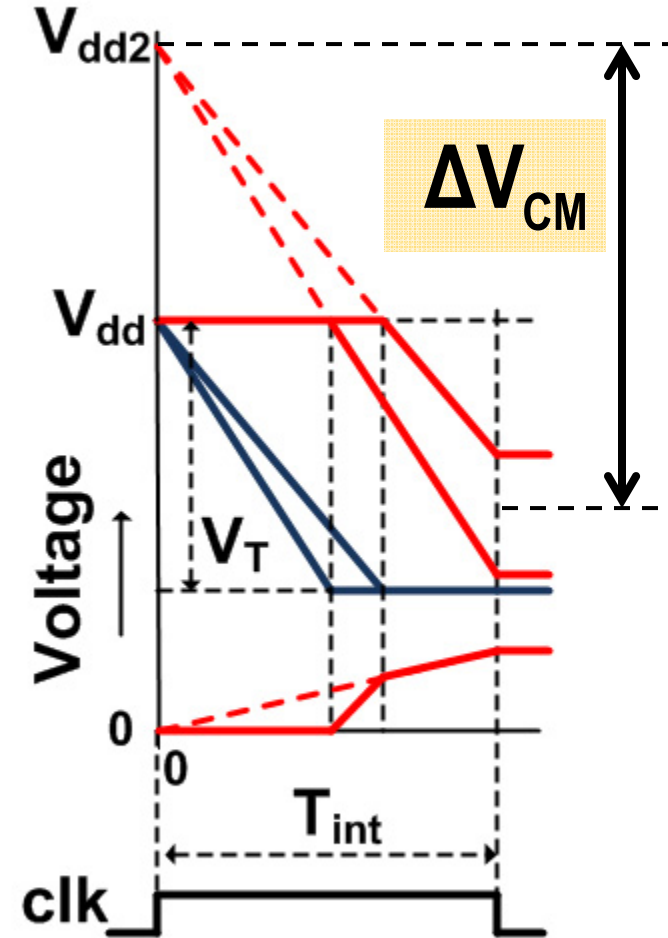
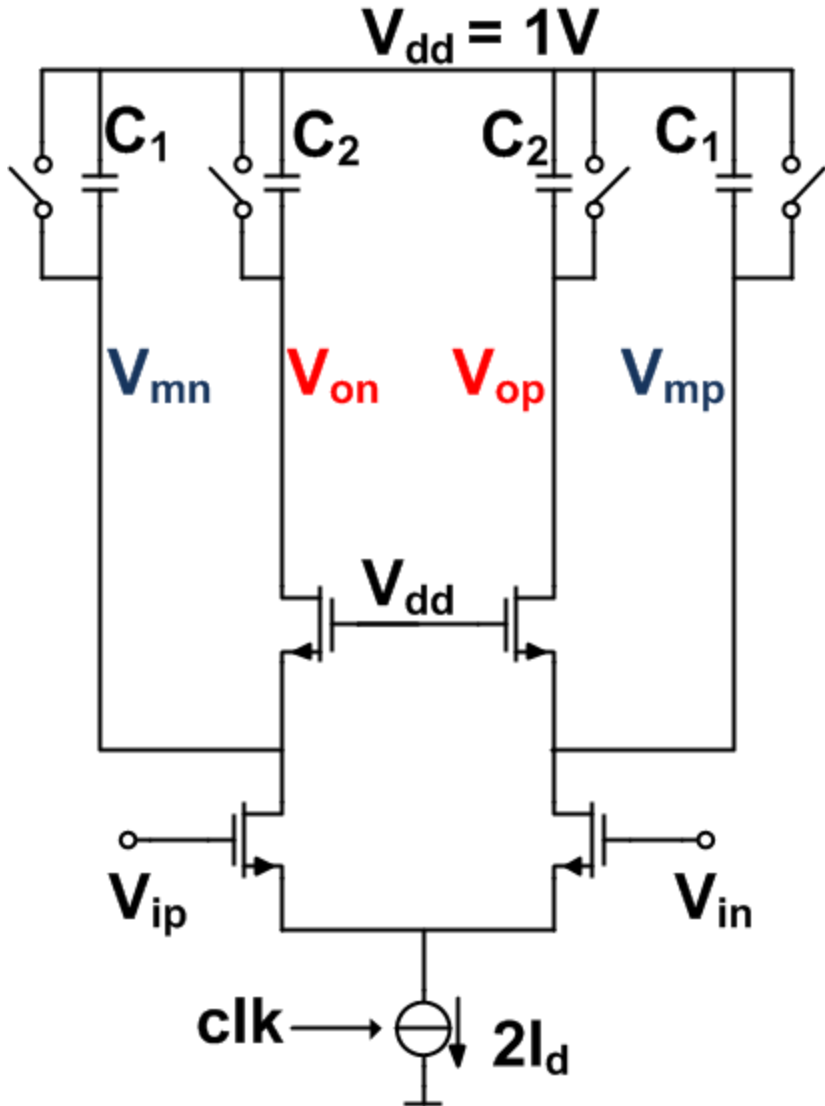
Operation principle (7/7)



Virtual boost of ΔV_{cm}



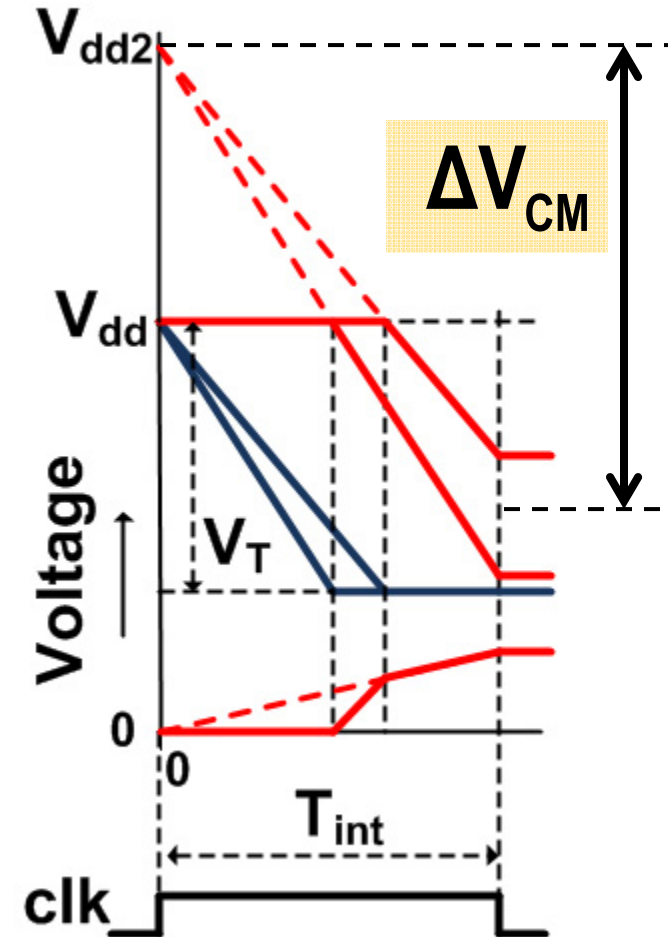
Virtual boost of ΔV_{cm}



Circuit Properties: Gain

Gain=16x can easily be realized

Virtual boost of ΔV_{cm} , without using a higher supply

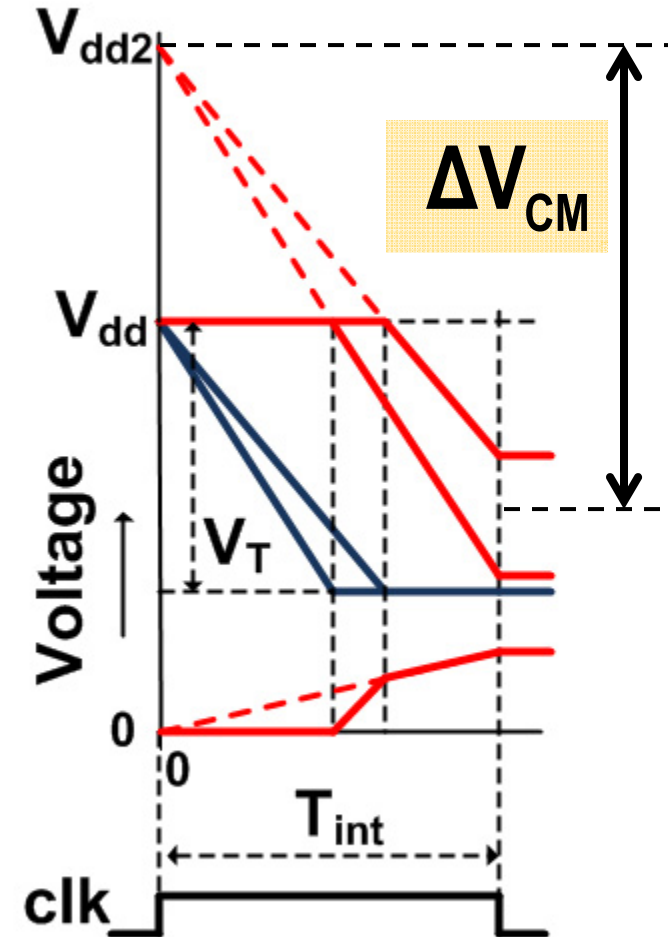


Circuit Properties: Noise Filtering

True integration during full T_{int}

- Integration not disrupted by cascodes turning on
- Continuous process

- Lowest input-referred noise
- Strongest noise filtering
 - Noise from Reference, DAC switches
 - Lowest noise bandwidth



Setting the Integration Time

Required: fixed integration time without jitter

Low-noise high-frequency clock is not available

- SAR is self-timed (asynchronous)**

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Required: fixed integration time without jitter

Low-noise high-frequency clock is not available

- SAR is self-timed (asynchronous)**

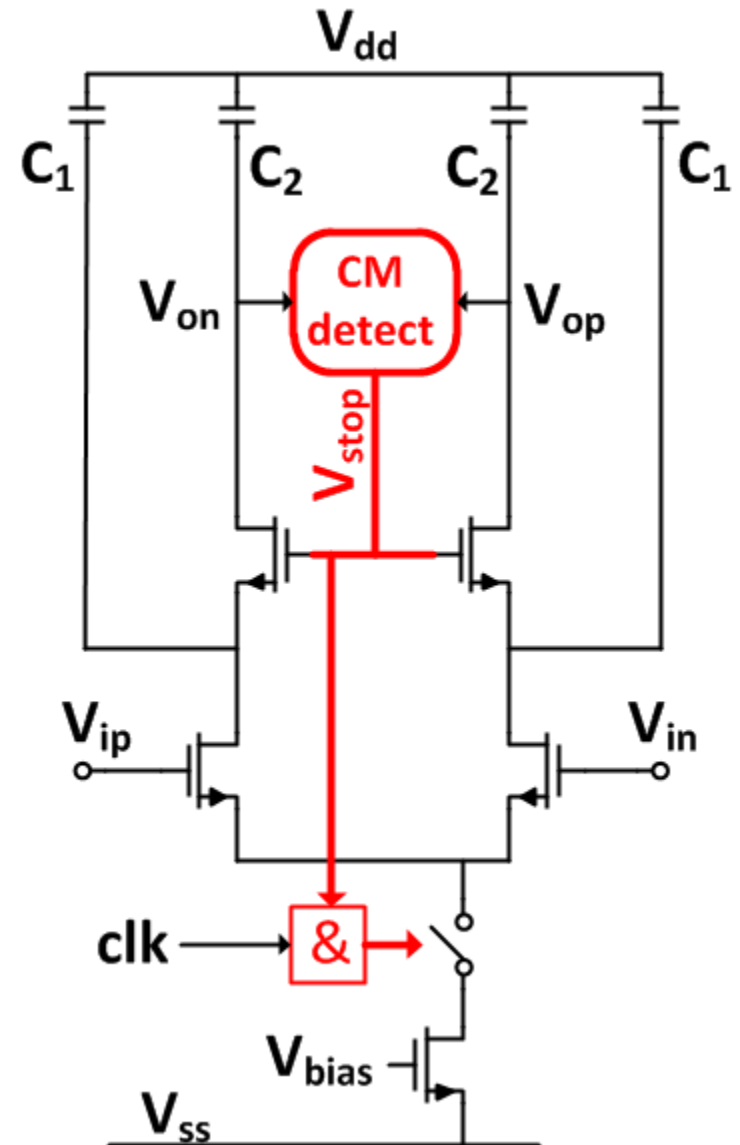
Use moving CM voltage of output of the residue amp.

Setting the Integration Time

Use CM detect
Lin [ISCAS 2011]

After crossing CM threshold:

- Switch off cascodes
 - disconnects C_2 (input stage 2)
- Switch off tail current



Setting the Integration Time

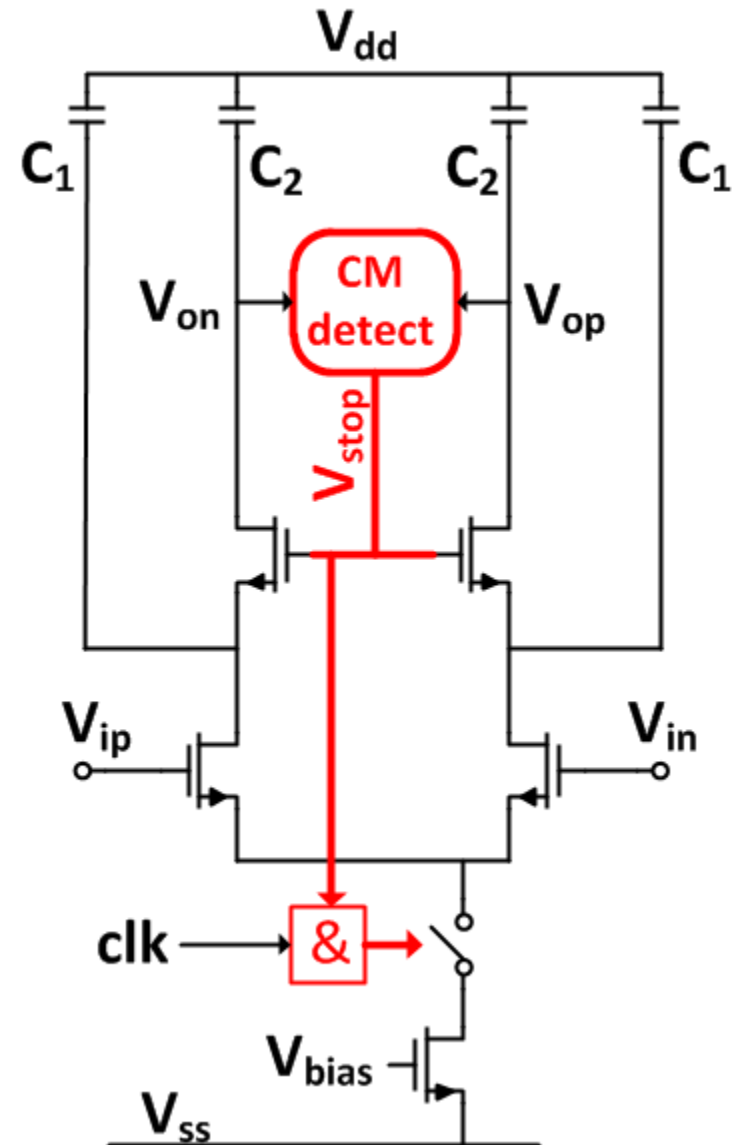
Use CM detect
Lin [ISCAS 2011]

After crossing CM threshold:

- Switch off cascodes
 - disconnects C_2 (input stage 2)
- Switch off tail current

Main Advantage:

- Use high CM slope of low-noise signals V_{op}/V_{on}



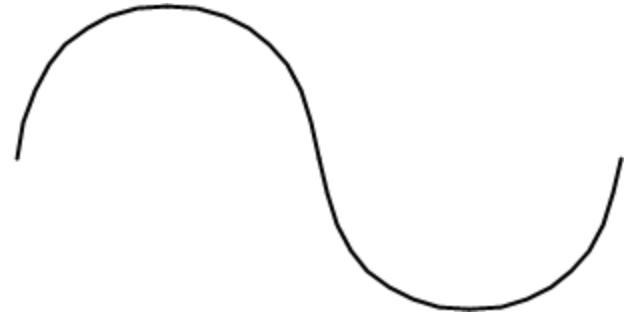
Improving Power Efficiency

Noise



- **ADC Architecture**
- **Noise Filtering using Integrators**

Large Signals



- **Reference Settling**
- **Reduced DAC Switching Energy**

Reference Generator

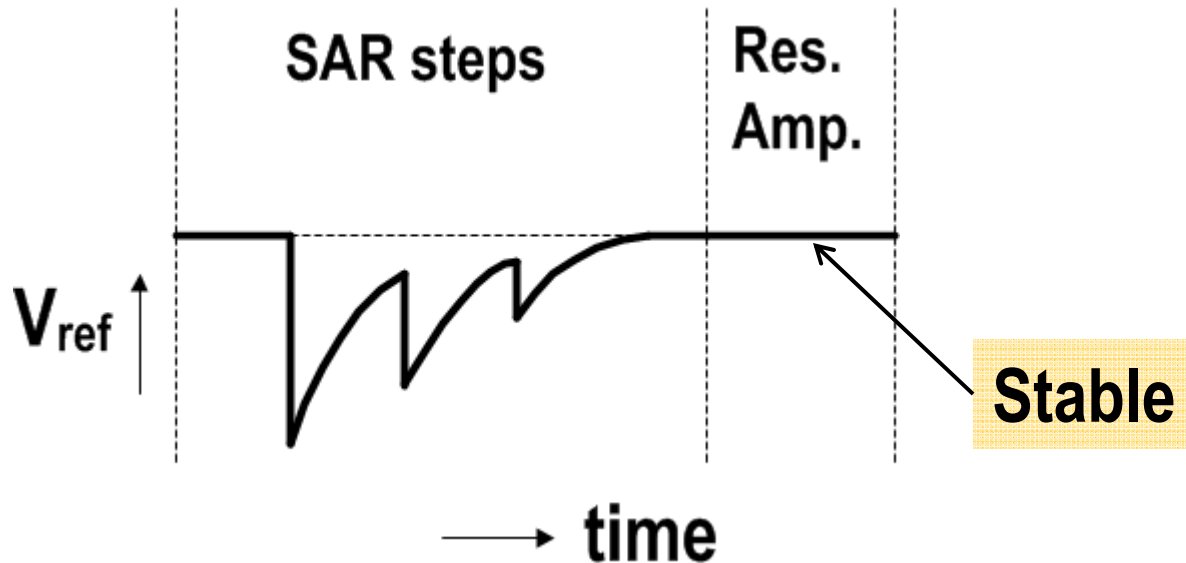
Industrial environment:

- Board voltages can not be used directly for V_{ref}
 - Too noisy due to crosstalk
 - Need good PSRR
- Use of board components should be avoided
- Use of large on-chip caps should be avoided

No large caps connected to V_{ref} :

Reference voltage WILL move during SAR phase

Limited Settling and Reduced Radix



Save power: allow settling of V_{ref} BETWEEN SAR steps

Would cause errors in SAR loop with Radix=2

DAC Radix: 1.7 \rightarrow 9 SAR steps for 7-bit resolution

Bias current reduction wrt settled-out: 2-3x

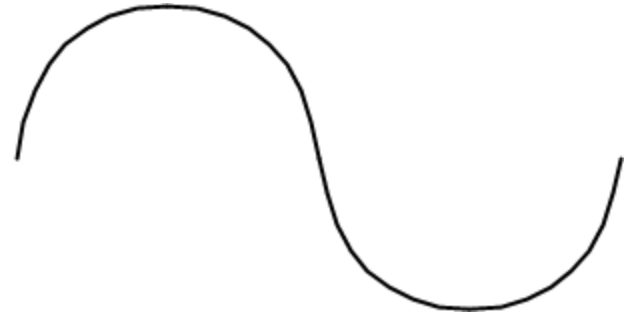
Improving Power Efficiency

Noise



- **ADC Architecture**
- **Noise Filtering using Integrators**

Large Signals



- **Reference Settling**
- **Reduced DAC Switching Energy**

Reducing DAC Switching Energy

Many techniques out there

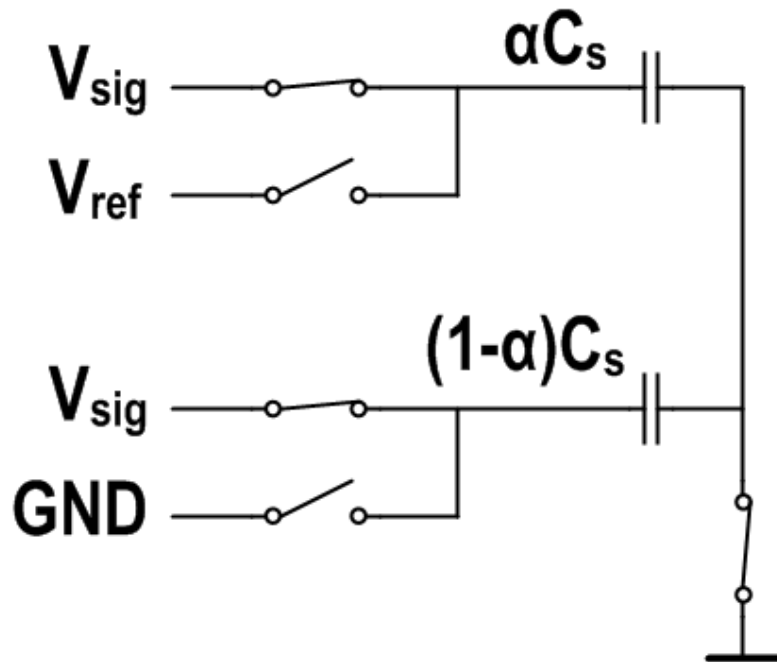
Split-capacitor technique

Ginsburg [ISCAS 2005]

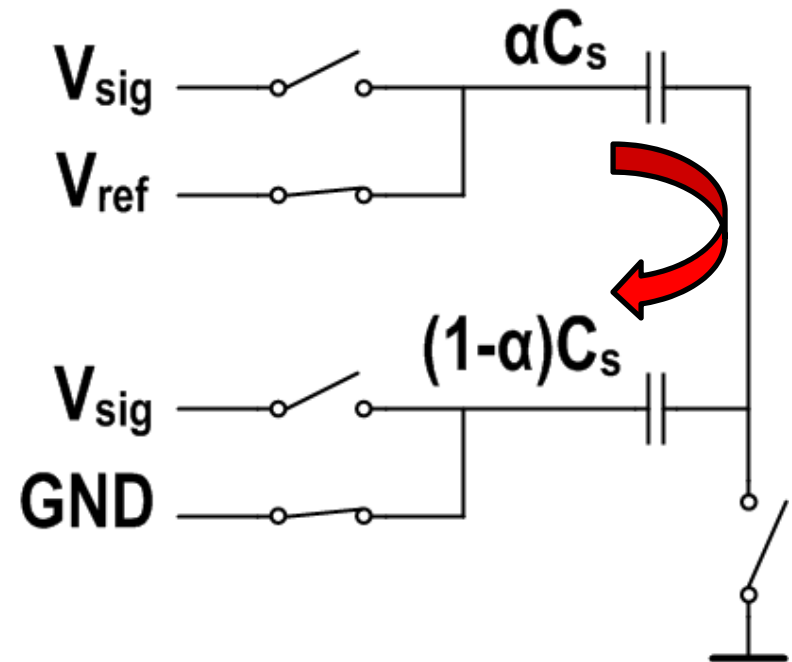
Modified DAC switching scheme

Interpolation takes Power

Track



Conversion

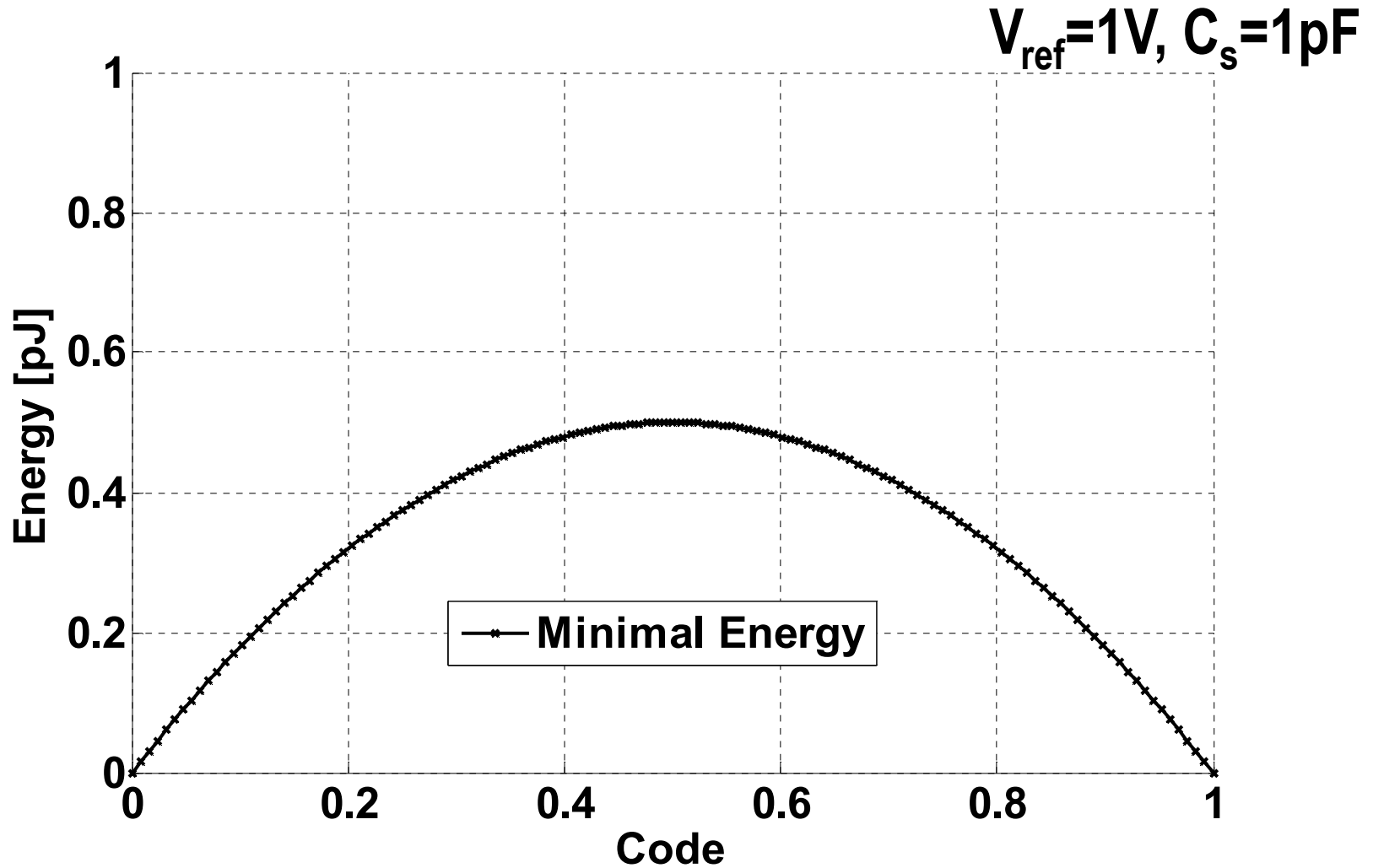


Only 2 reference voltages (V_{ref} / GND) available

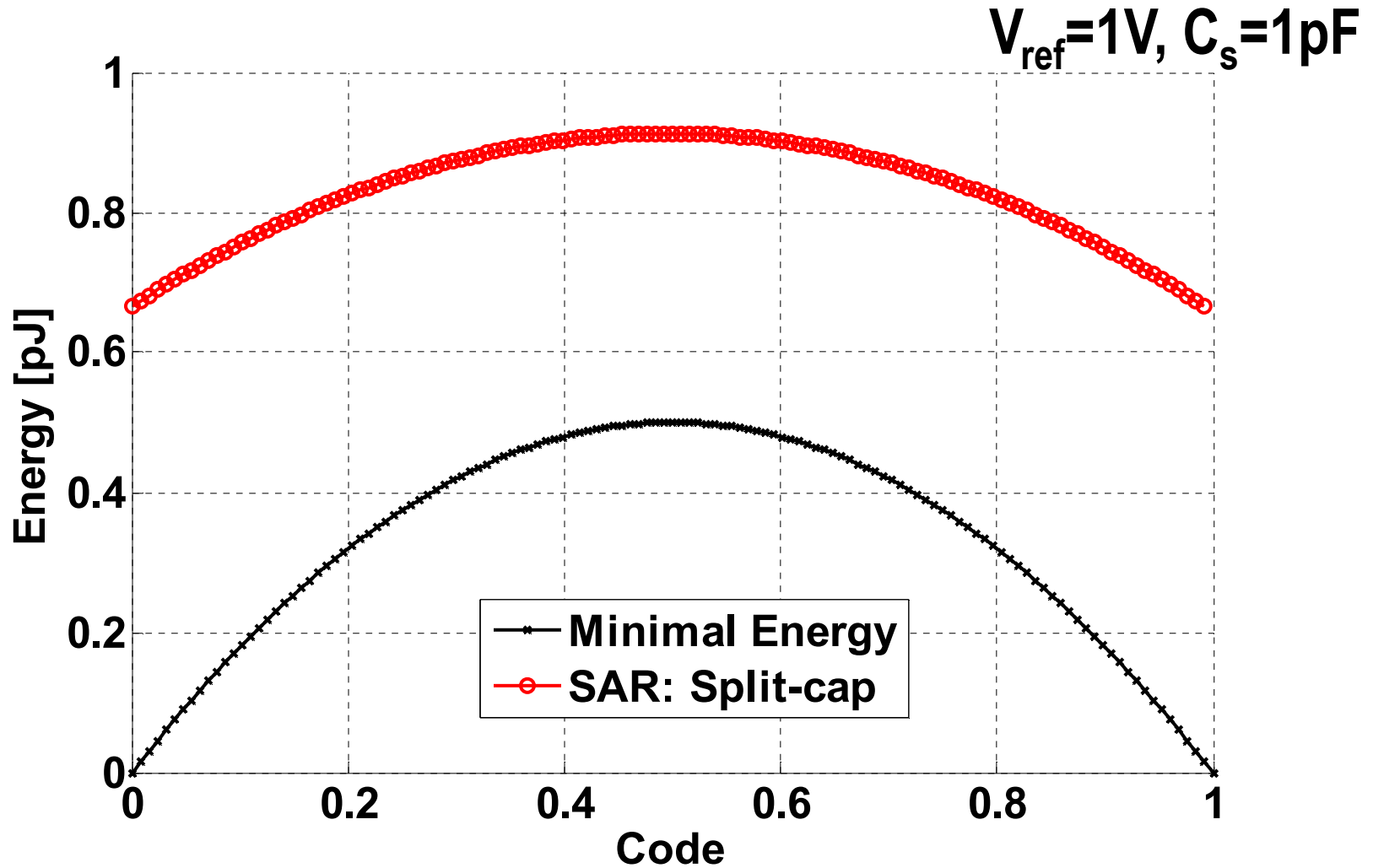
7-bit DAC: interpolation is required

Interpolation takes power from V_{ref}

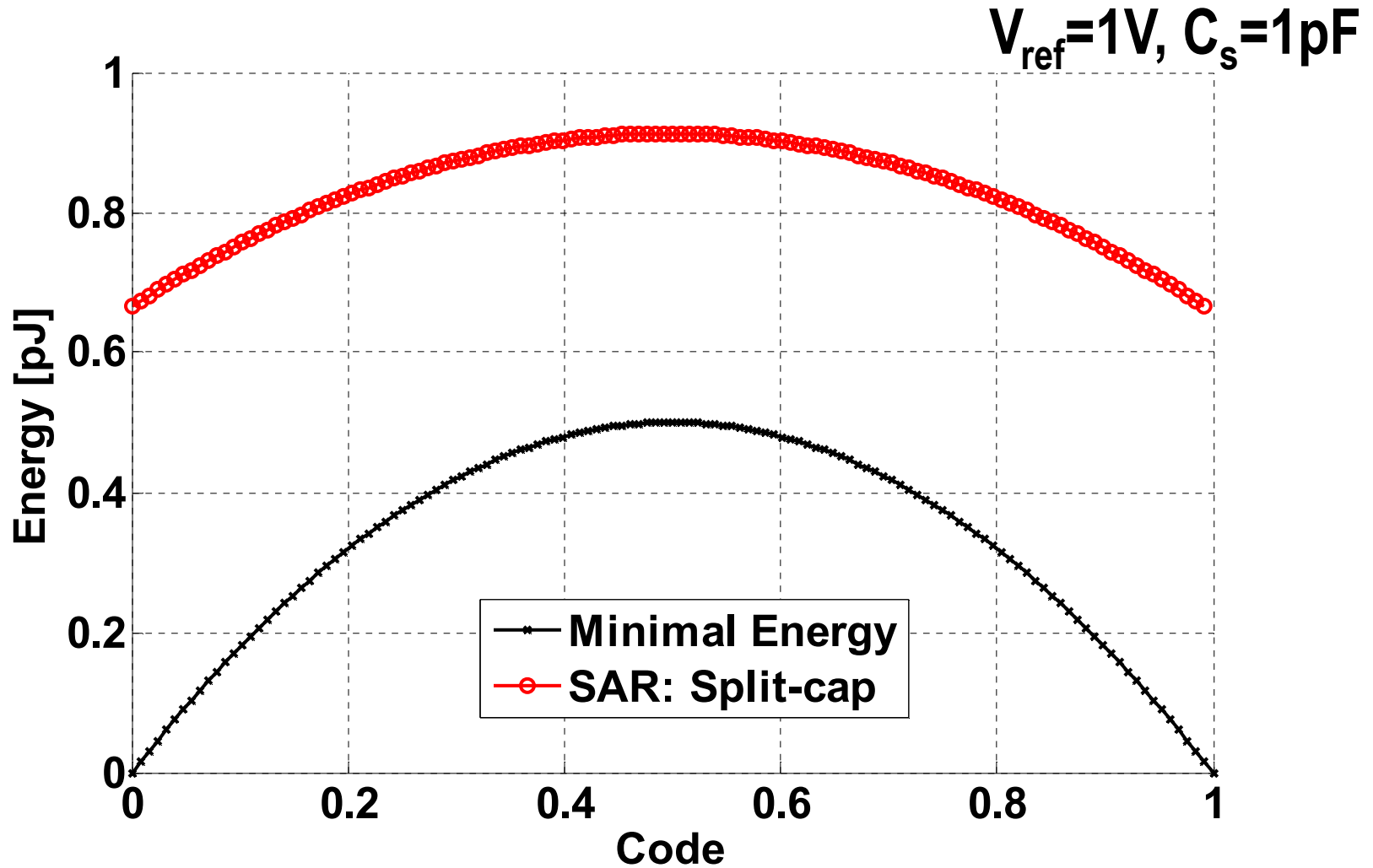
Minimal Energy vs DAC Code



Energy vs DAC Code



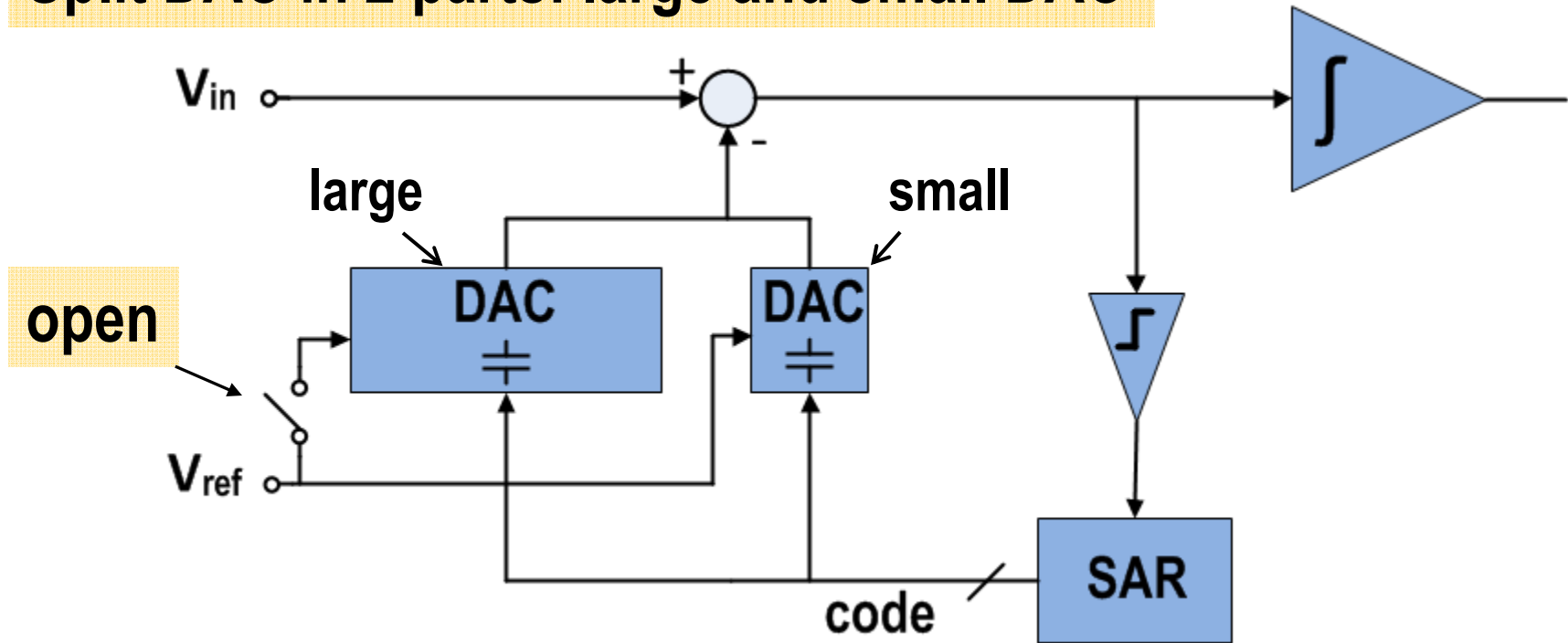
Energy vs DAC Code



Idea: First few SAR steps with small caps

First Few SAR Steps

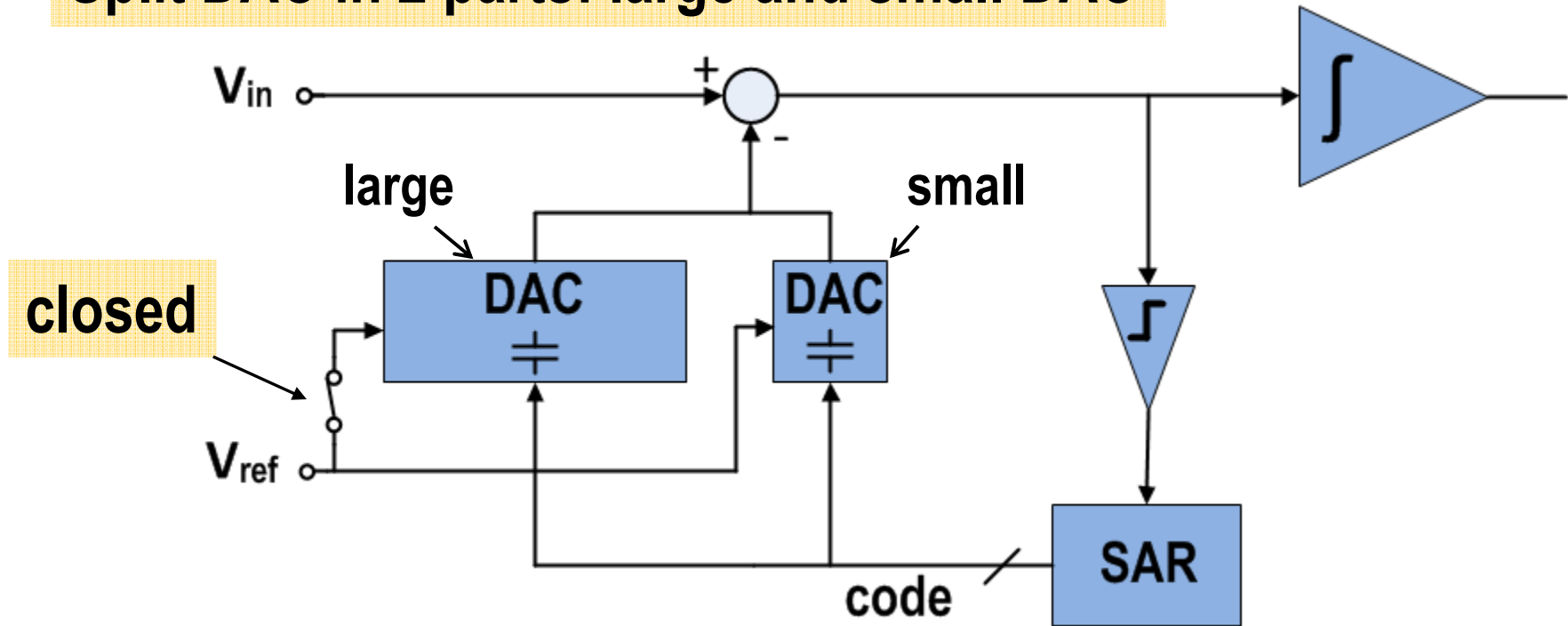
Split DAC in 2 parts: large and small DAC



Small DAC produces MSBs
Only small DAC draws charge from V_{ref}

Remaining SAR Steps

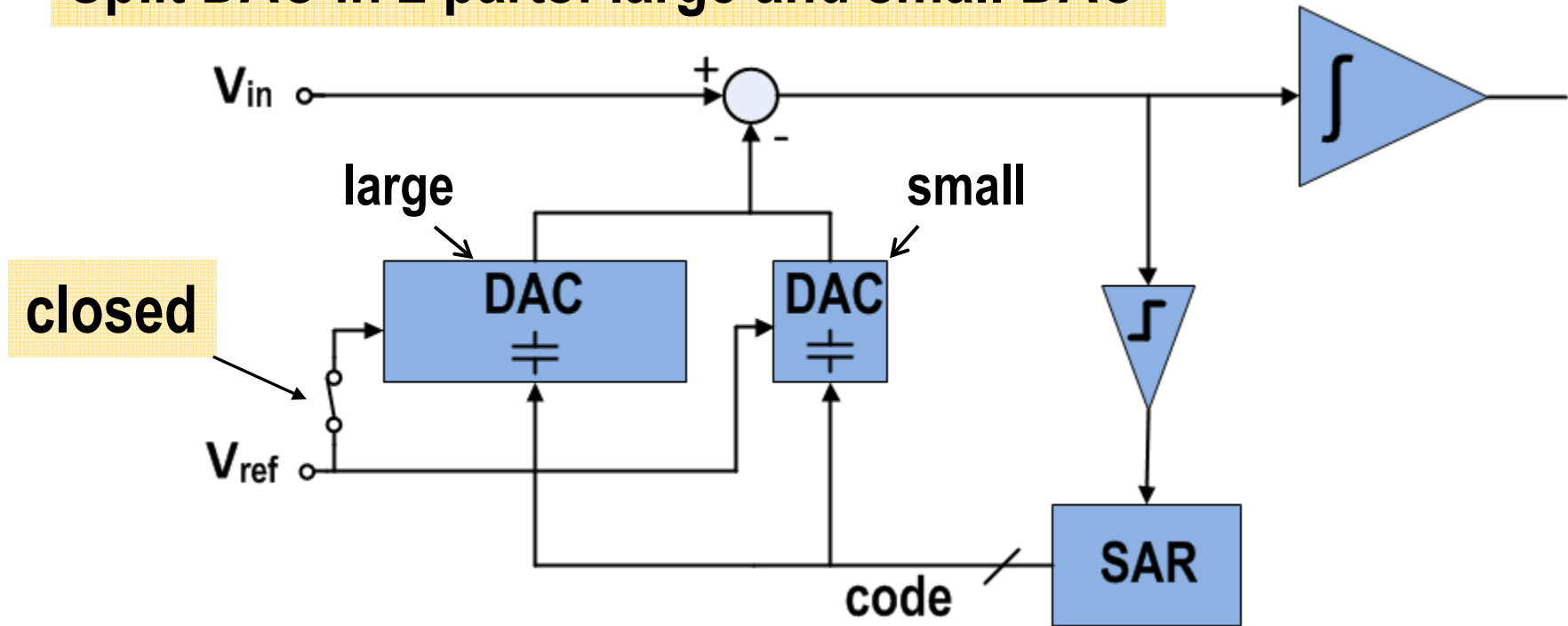
Split DAC in 2 parts: large and small DAC



Both DACs connected to V_{ref} , receiving same code

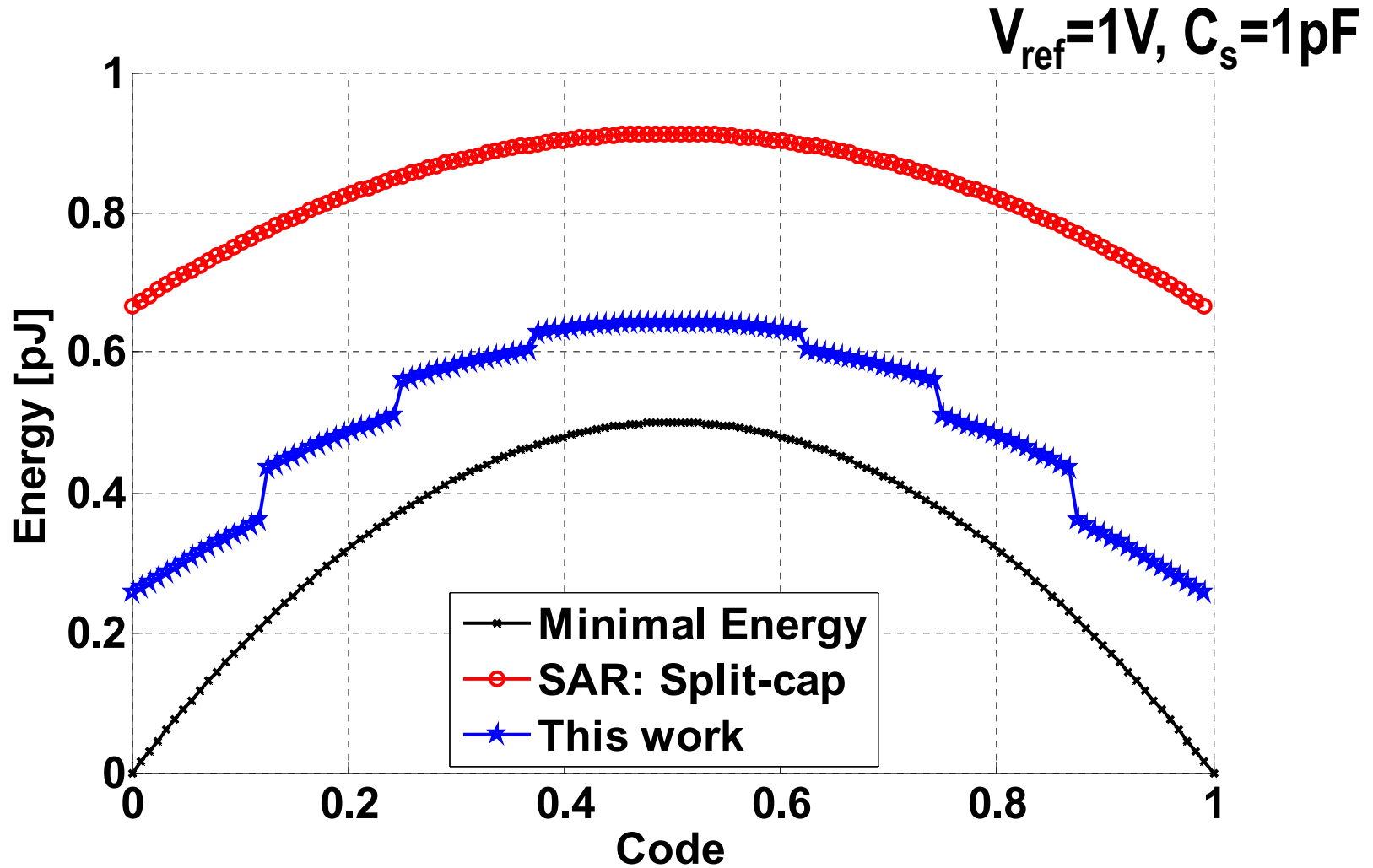
Remaining SAR Steps

Split DAC in 2 parts: large and small DAC



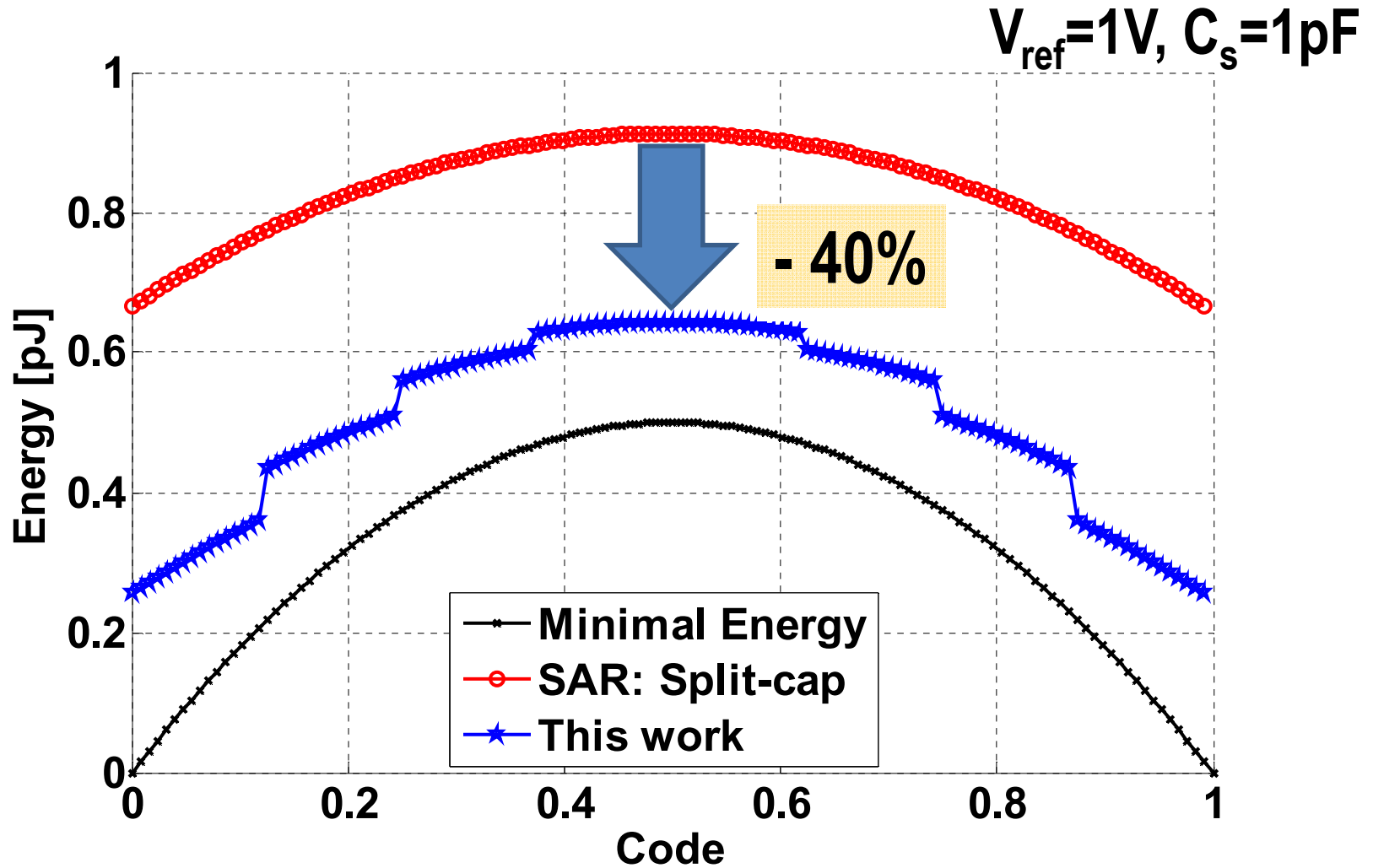
Both DACs connected to V_{ref} , receiving same code
Aligned DACs: enabling large DAC is transparent to SAR
Any mismatch between DACs: Overrange ($R=1.7$)

Energy vs DAC Code



Large DAC enabled after 3rd comparator decision

Energy vs DAC Code

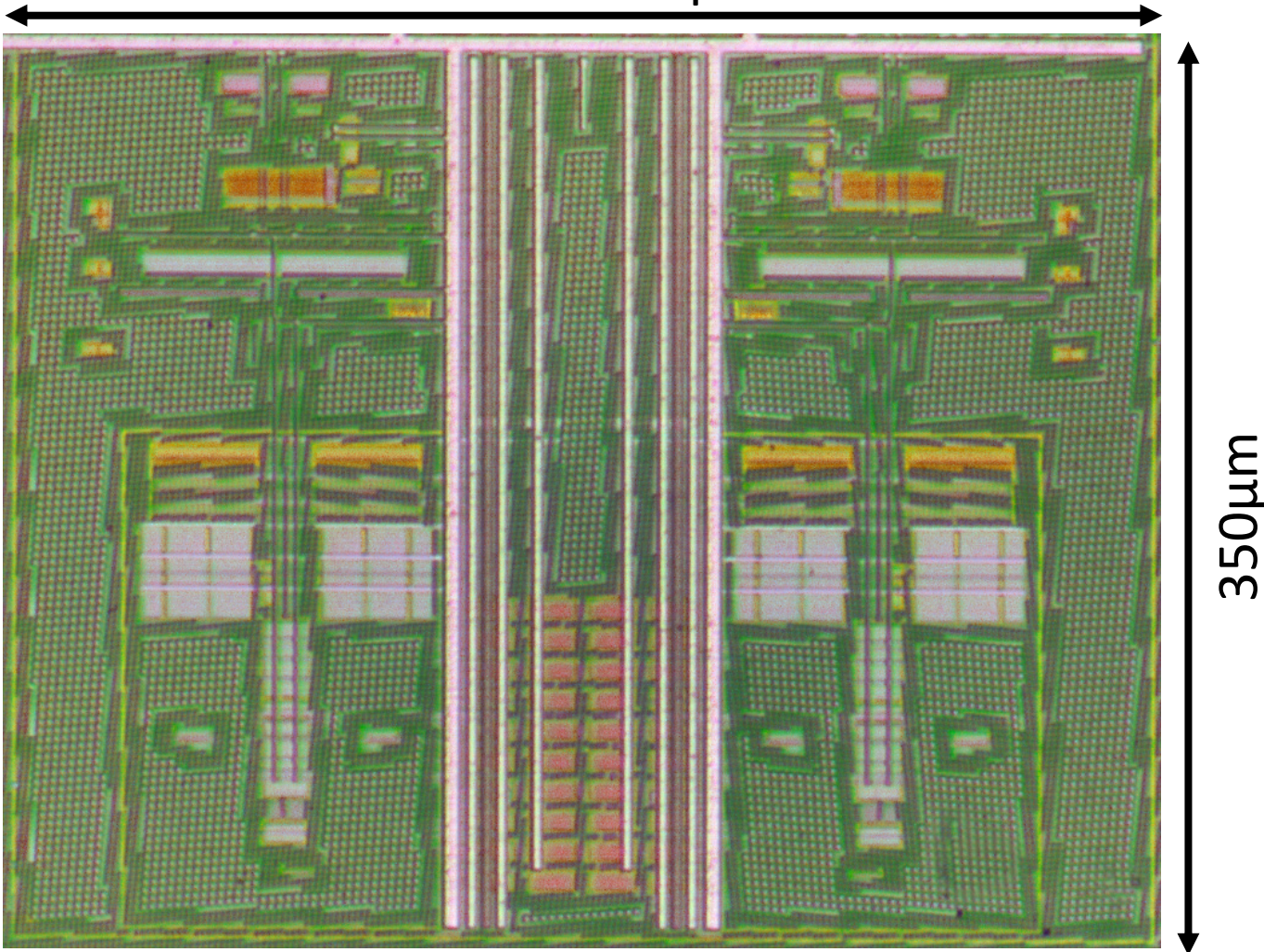


Large DAC enabled after 3rd comparator decision

Chip micrograph

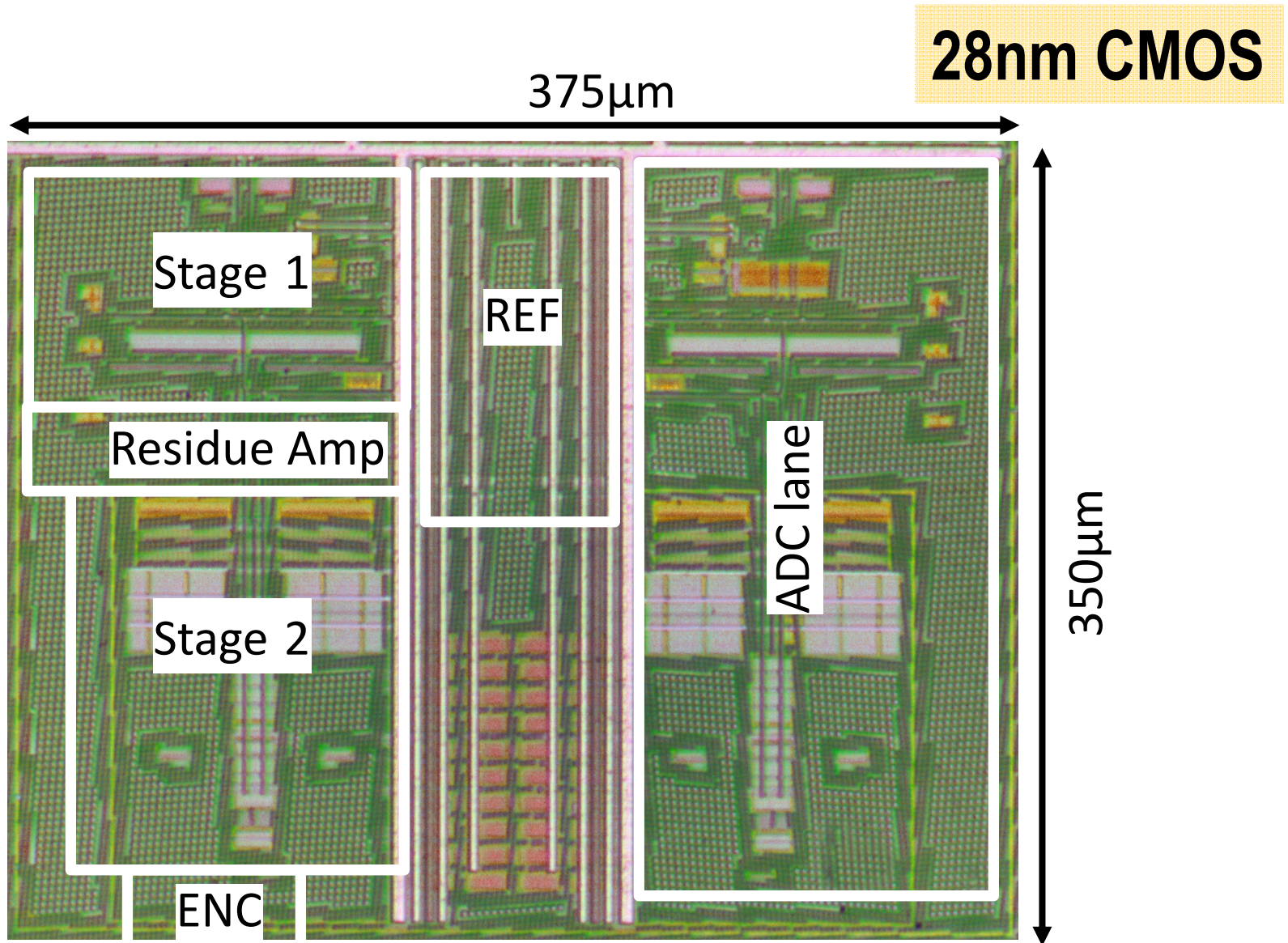
28nm CMOS

375 μ m



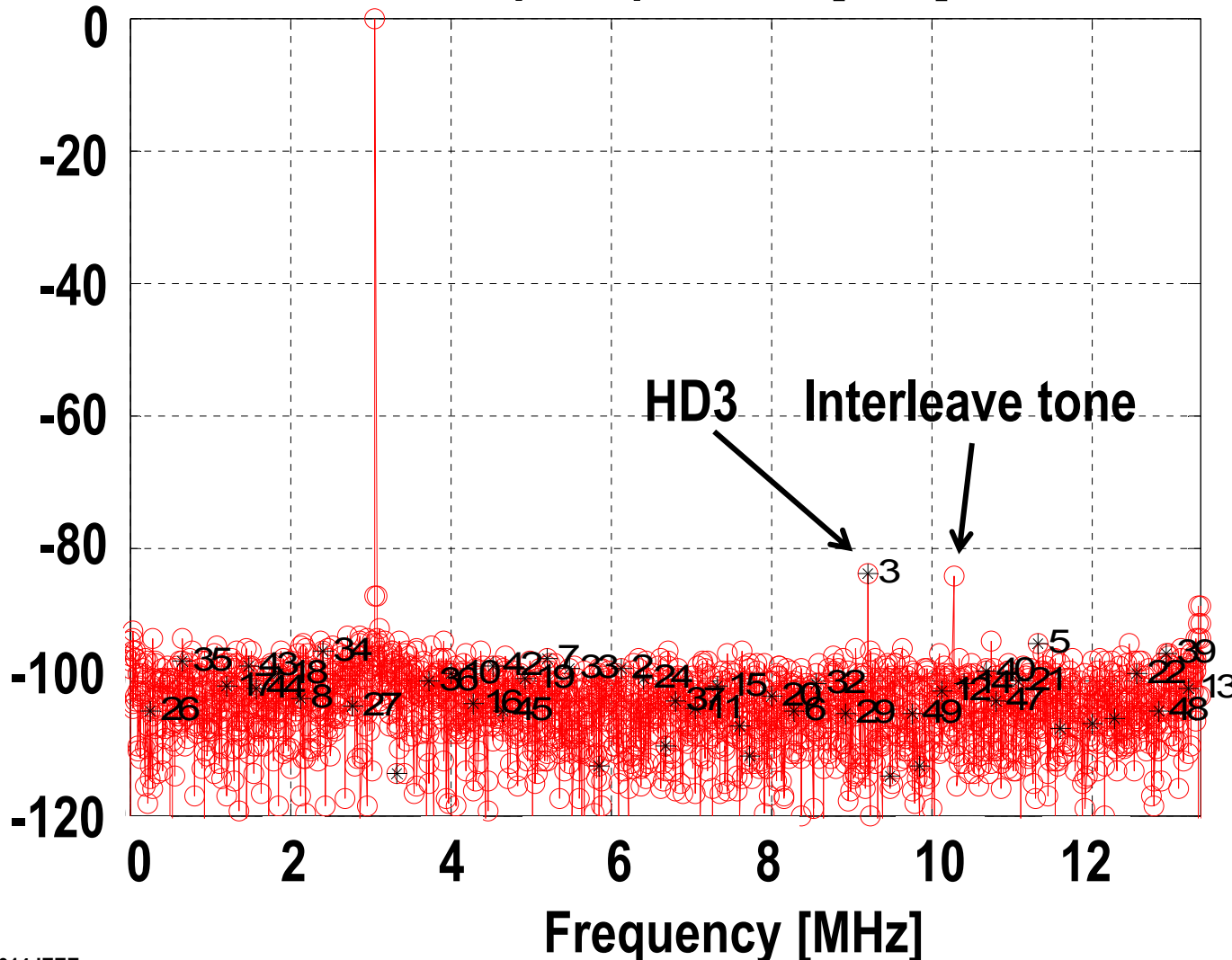
350 μ m

Chip micrograph



FFT of output data – $F_{\text{sig}}=3\text{MHz}$

Output Spectrum [dBc]

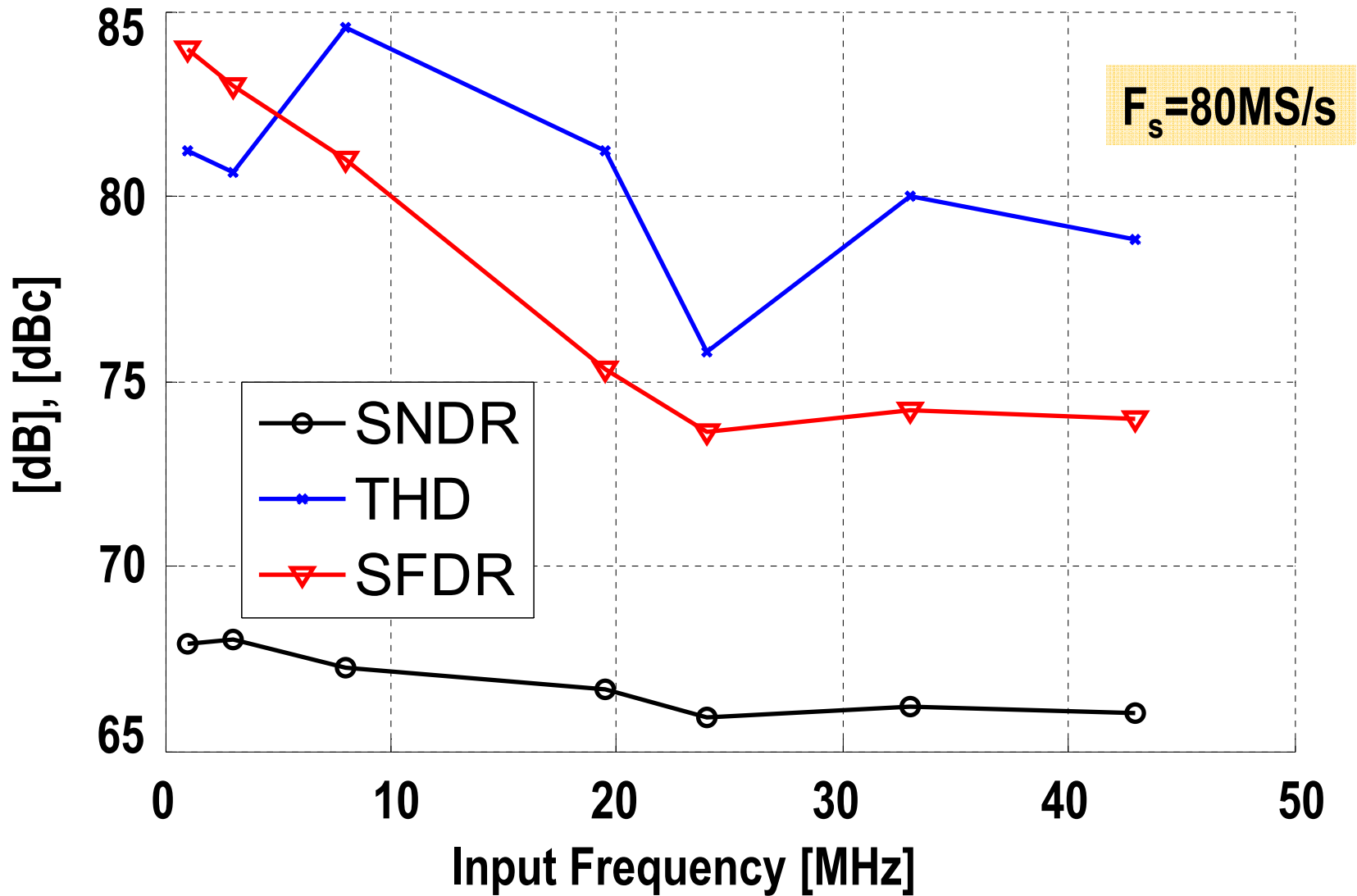


SNDR=68dB

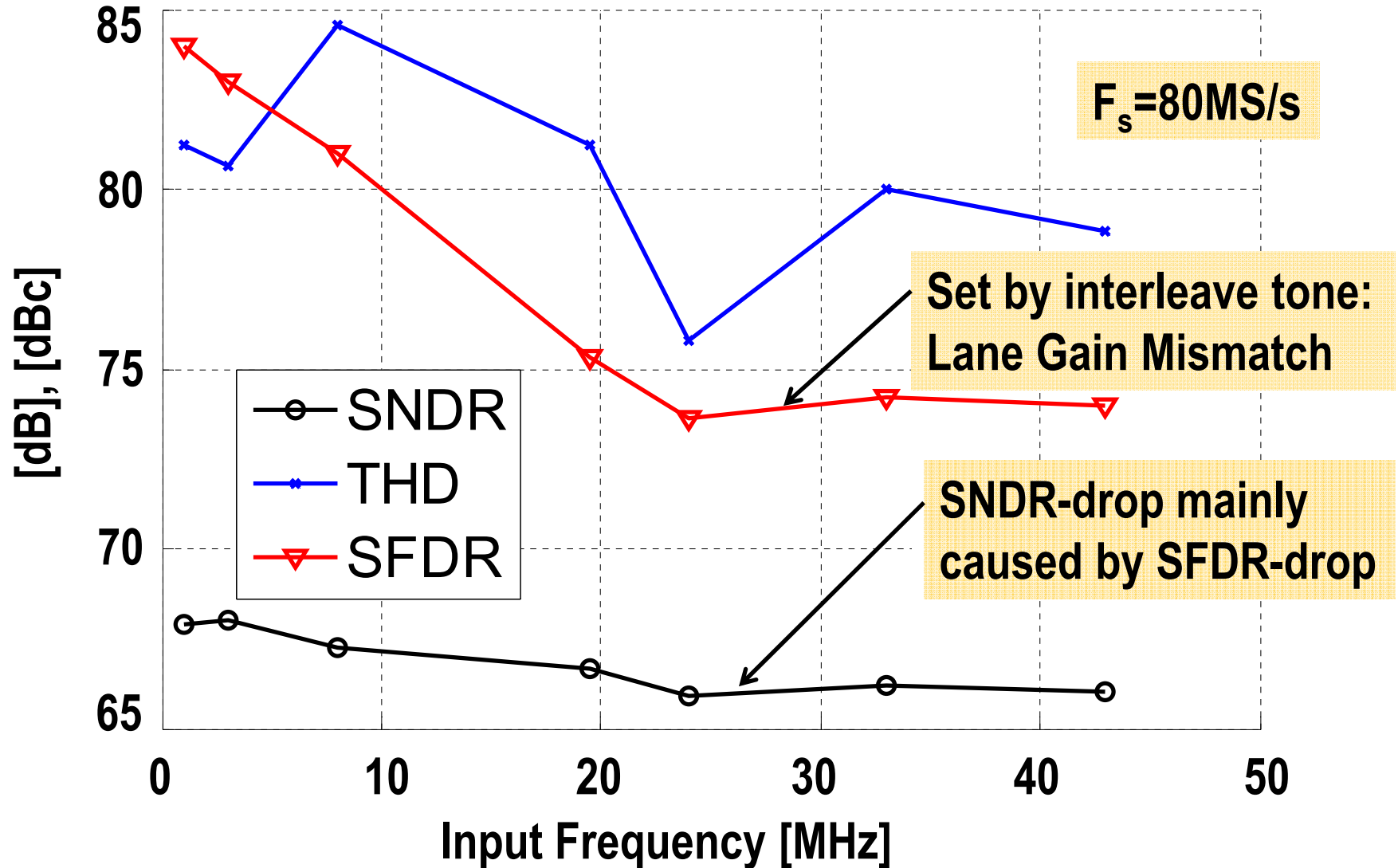
$F_s=80\text{MS/s}$

3x decimation
of output data
→ $F_s = 13.3\text{MHz}$

Performance vs F_{sig}



Performance vs F_{sig}



Comparison

	Kapusta ISSCC 2013	Morie ISSCC 2013	Verbruggen ISSCC 2012	This work
Technology	65nm CMOS	90nm CMOS	40nm CMOS	28nm CMOS
Architecture	SAR	SAR	SAR-assist. Pipelined	SAR-assist. Pipelined
Supply [V]	1.2	1.2	1.1	1.0 / 1.8
ADC FS [V_{ppd}]	2.4	2.2	-	1.4
F_s [MS/s]	80	50	250	80
Peak SNDR [dB]	73.6	71	58.7	68
Power [mW]	31.1	4.2	1.7	1.5
Walden FoM [fJ/conv-st]	99.4	29.7	9.7	9.1
Schreier FoM [dB]	164.7	168.7	167.4	172.3
Ref. included	No	No	No	Yes

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Ref. included	No	No	No	Yes

Summary

- **80MS/s 11-bit ENOB ADC**
- **28nm CMOS**
- **on-chip Reference, no external components**
- **1.5mW**

- **Pipelined SAR ADC**
- **Noise Filtering using Integrators**

- **Reference Settling**
- **Reduced DAC Switching Energy**

Beyond State-of-the-Art FoM

Thank you

A 100MS/s, 10.5-Bit, 2.46mW Comparator-less Pipeline ADC Using Self-biased Ring Amplifiers

Yong Lim^{1, 2}, Michael P. Flynn¹

¹University of Michigan, Ann Arbor, MI

²Samsung Electronics, Yongin, Korea

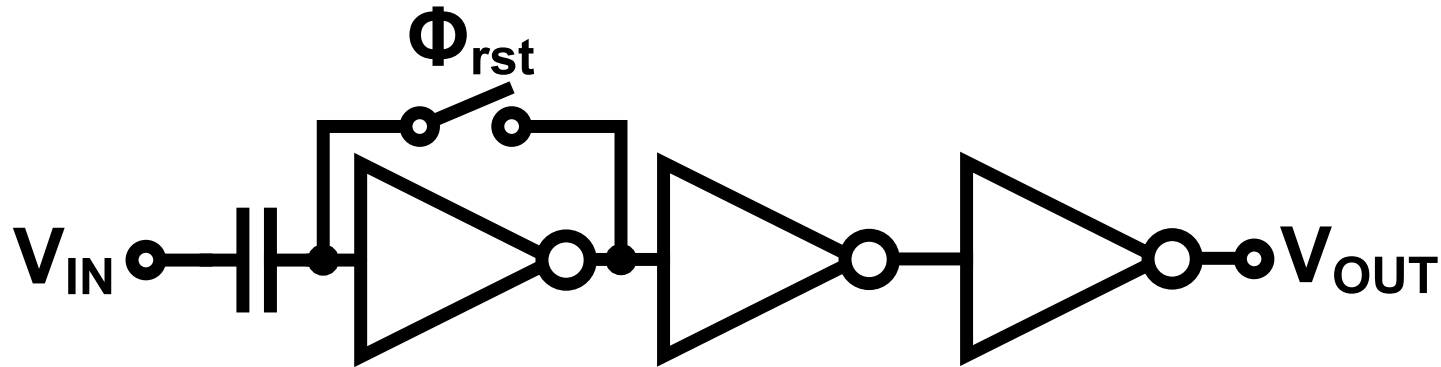
Key Contributions

- **Self-biased ring amplifier**
 - Practical and more power efficient
- **Improved auto-zero switching**
 - Eliminates parasitic capacitor gain error
- **Comparator-less 1.5b pipeline ADC stage**
- ➔ **Prototype ADC**
 - 44.5fJ/conv-step @100MS/s

Ring Amplifier

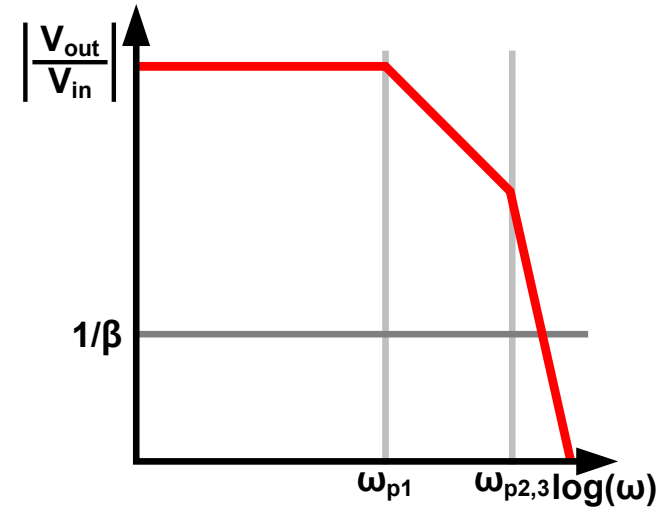
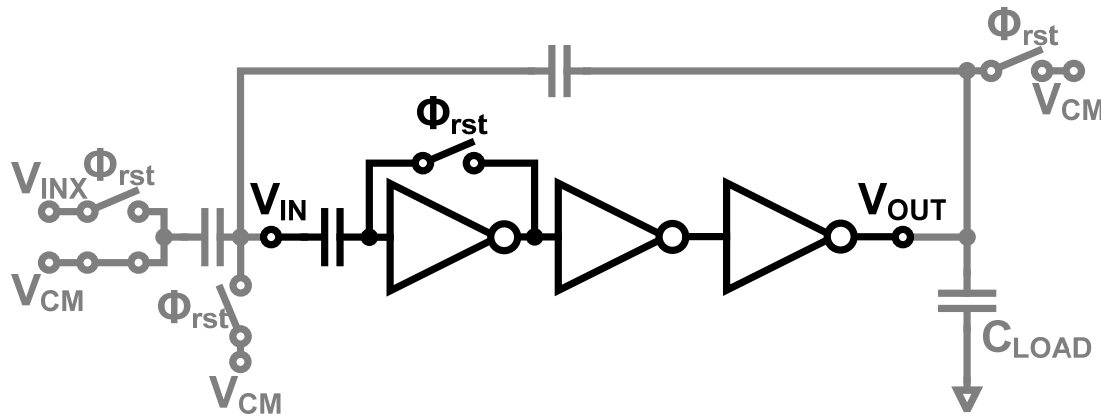
[Hershberg, ISSCC 2012]

Offset Canceled Three-stage Inverter



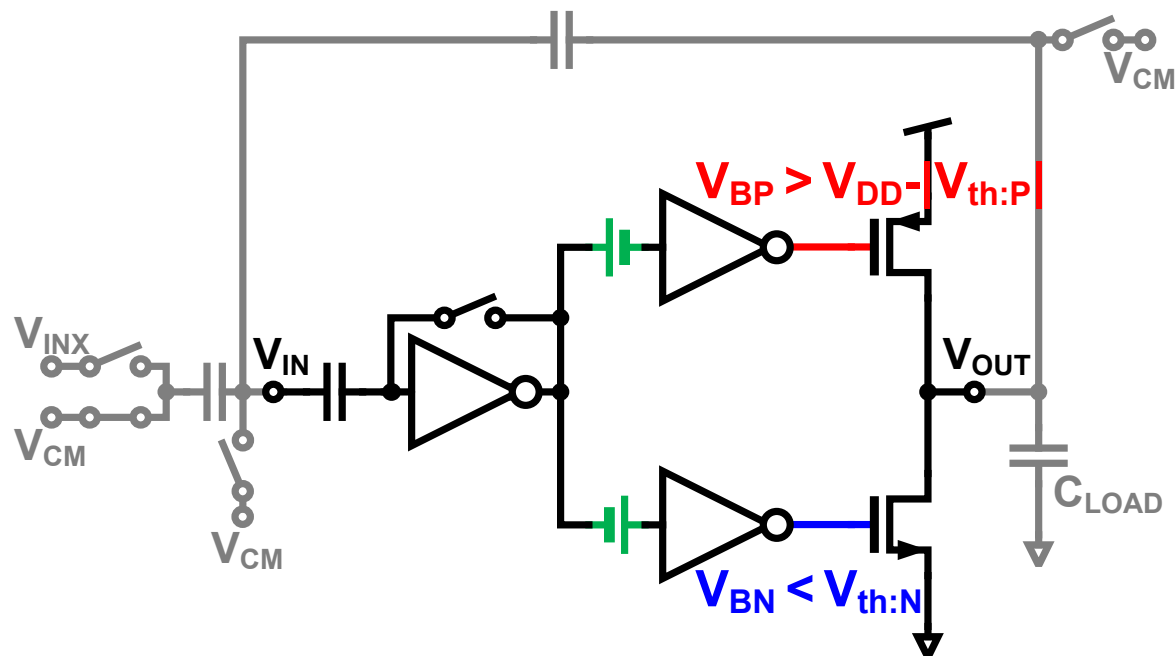
- Gain 😊
- Stability ??

Three-stage Inverter in Feedback



➤ Stability 😞 ➔ Ring Oscillator

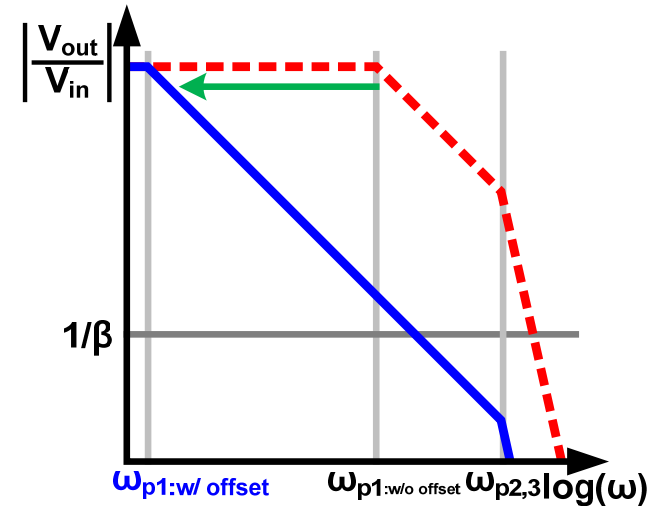
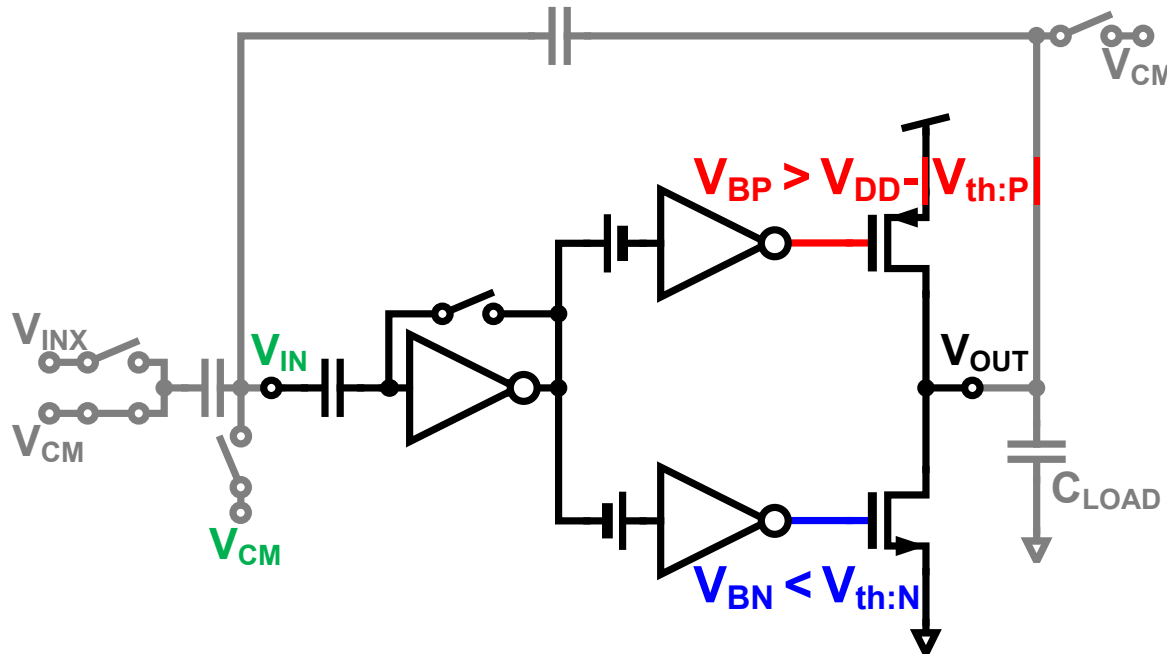
Stabilized Three-stage Inverter



➤ Split 2nd stage and apply offsets

[Hershberg, ISSCC 2012]

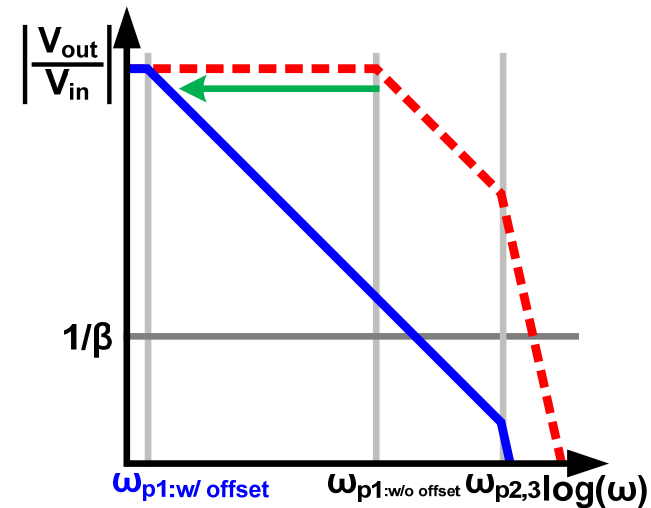
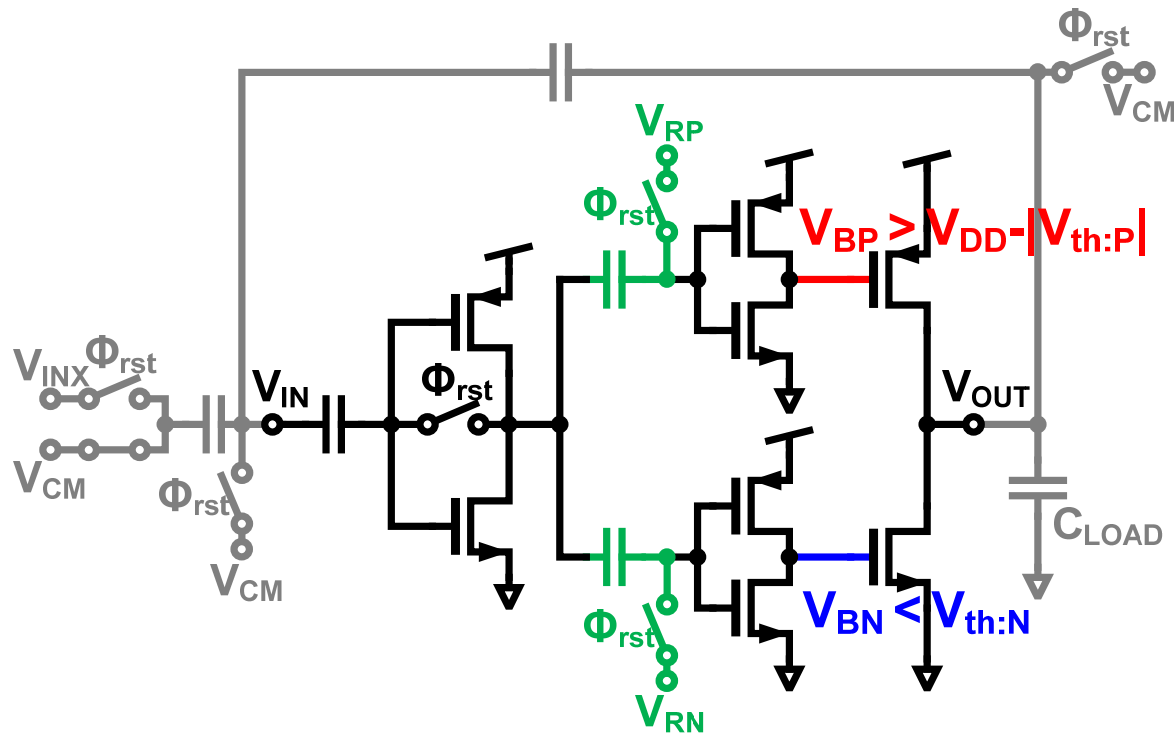
Stabilized Three-stage Inverter



- 3rd stage is in sub-threshold for $V_{IN} \approx V_{CM}$
- ➔ Output stage resistance increases dramatically

[Hershberg, ISSCC 2012]

Ring Amplifier – Practical Circuit

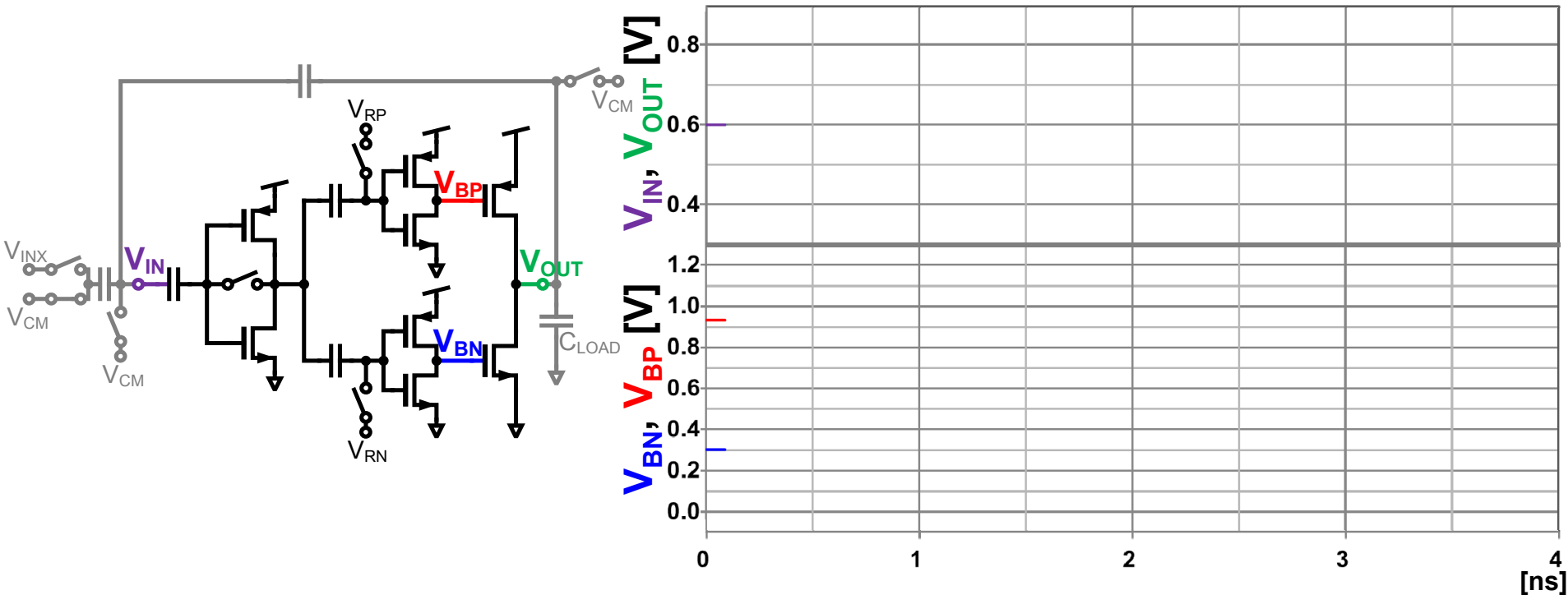


[Hershberg, ISSCC 2012]

Ring Amplifier Stabilization Criteria

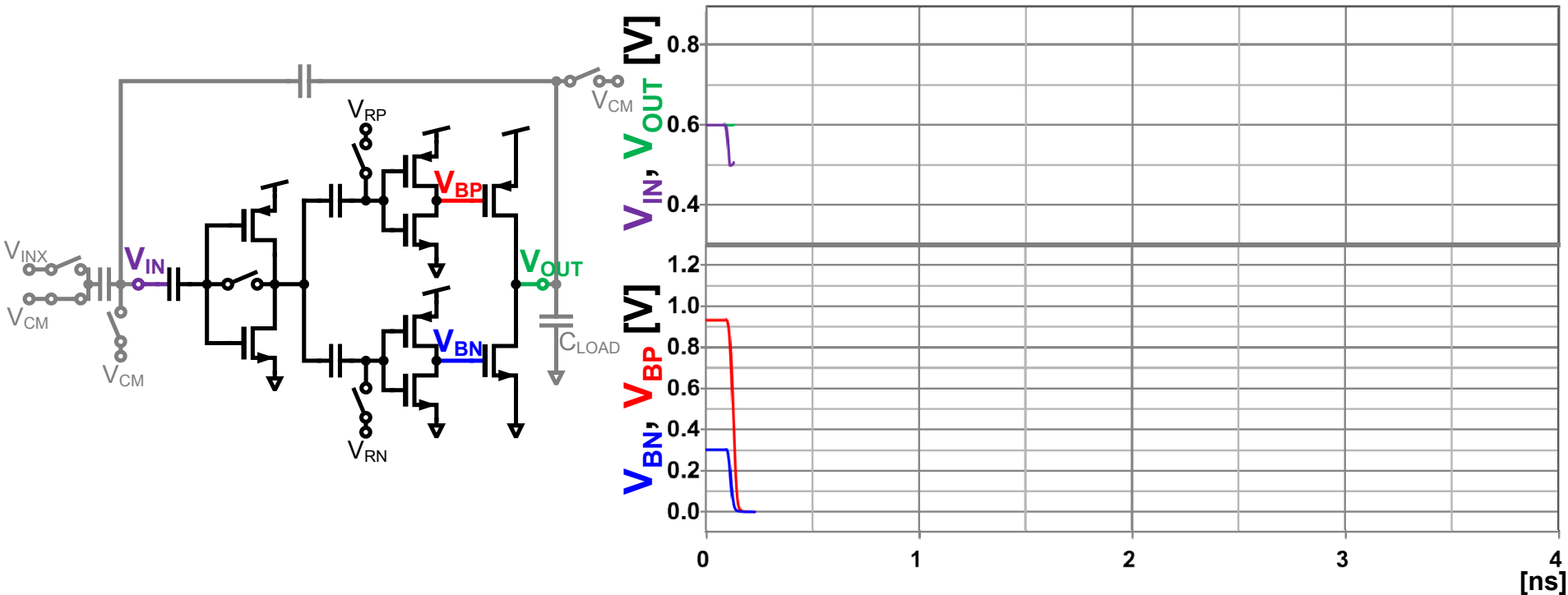
- **Small signal Positive phase margin**
 - Necessary, but not sufficient
- **Slewing current dramatically changes around the target settling point**
 - ➔ Need to check large signal behavior

Ring Amplifier Large Signal Behavior



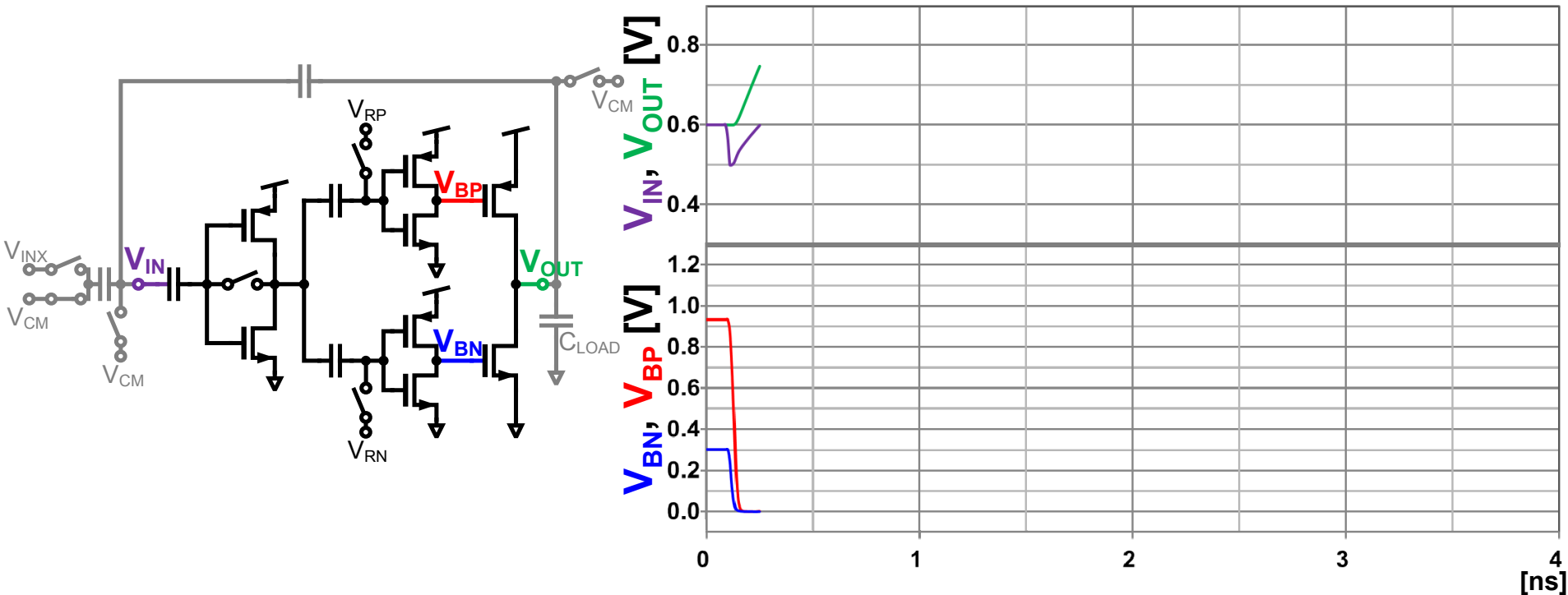
➤ Bias point

Ring Amplifier Large Signal Behavior



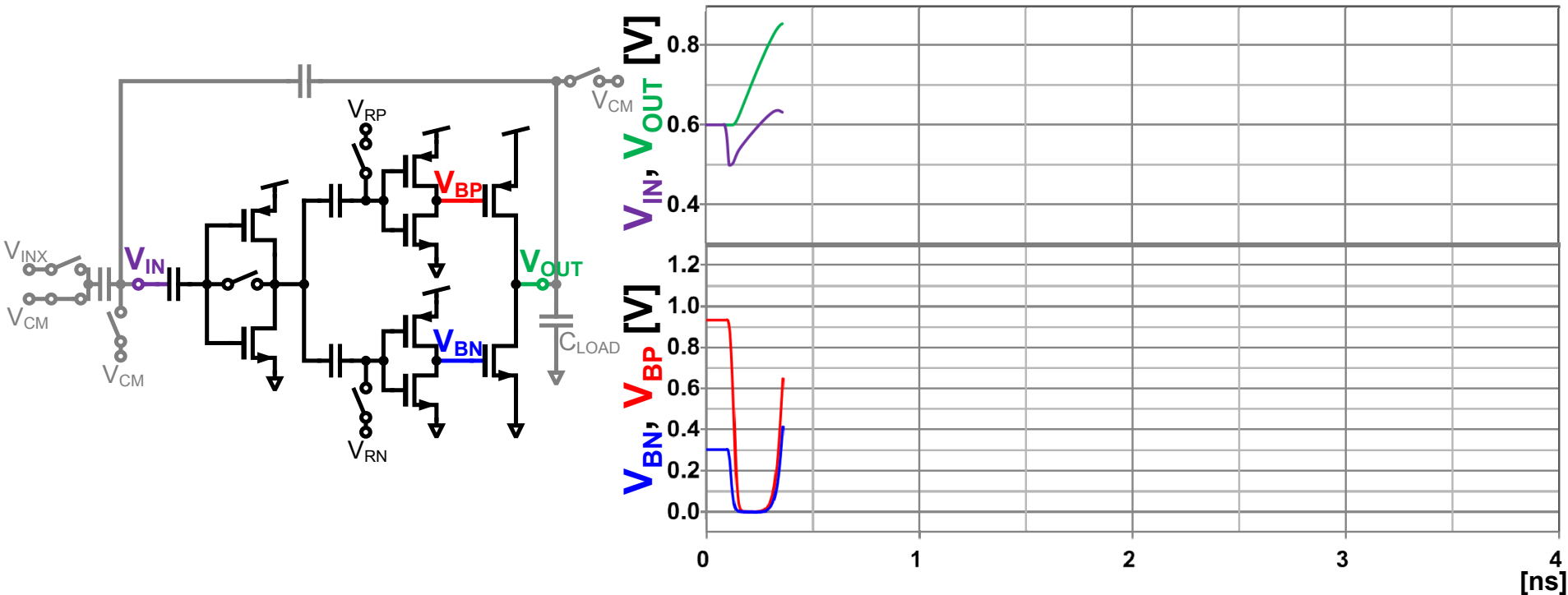
➤ Slew

Ring Amplifier Large Signal Behavior



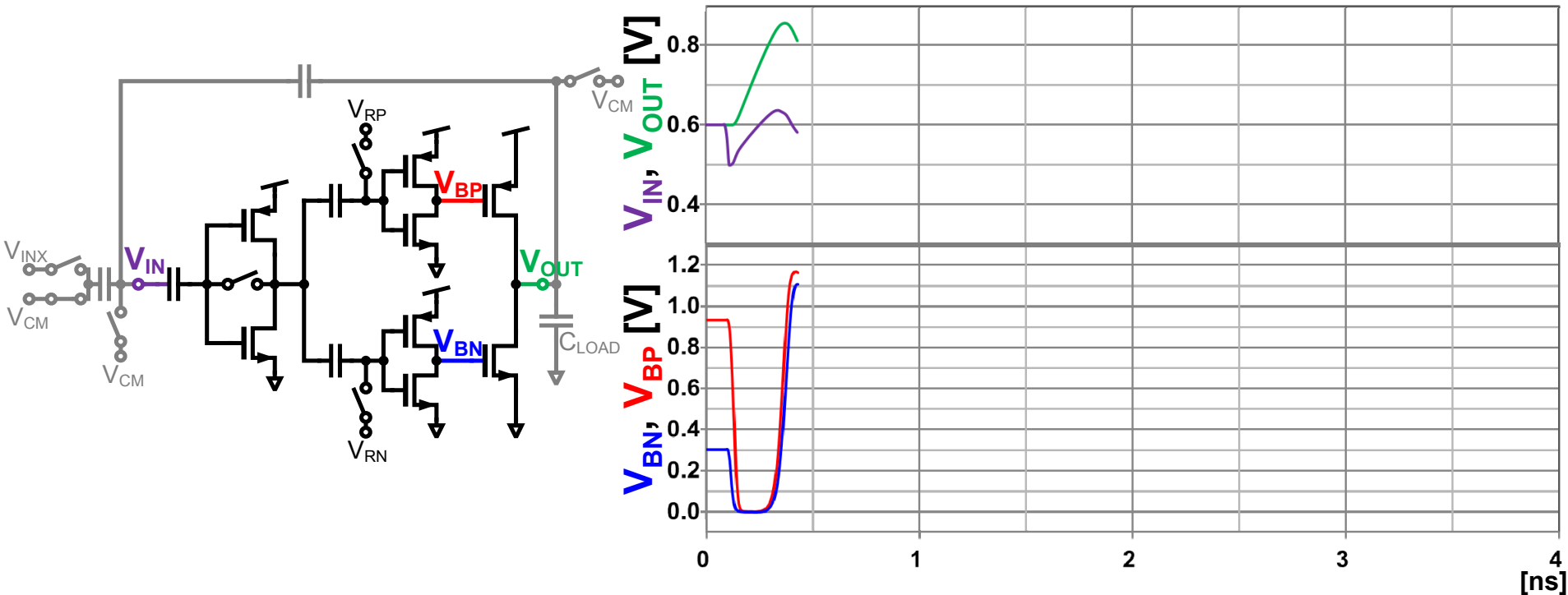
➤ Slew → finite response time

Ring Amplifier Large Signal Behavior



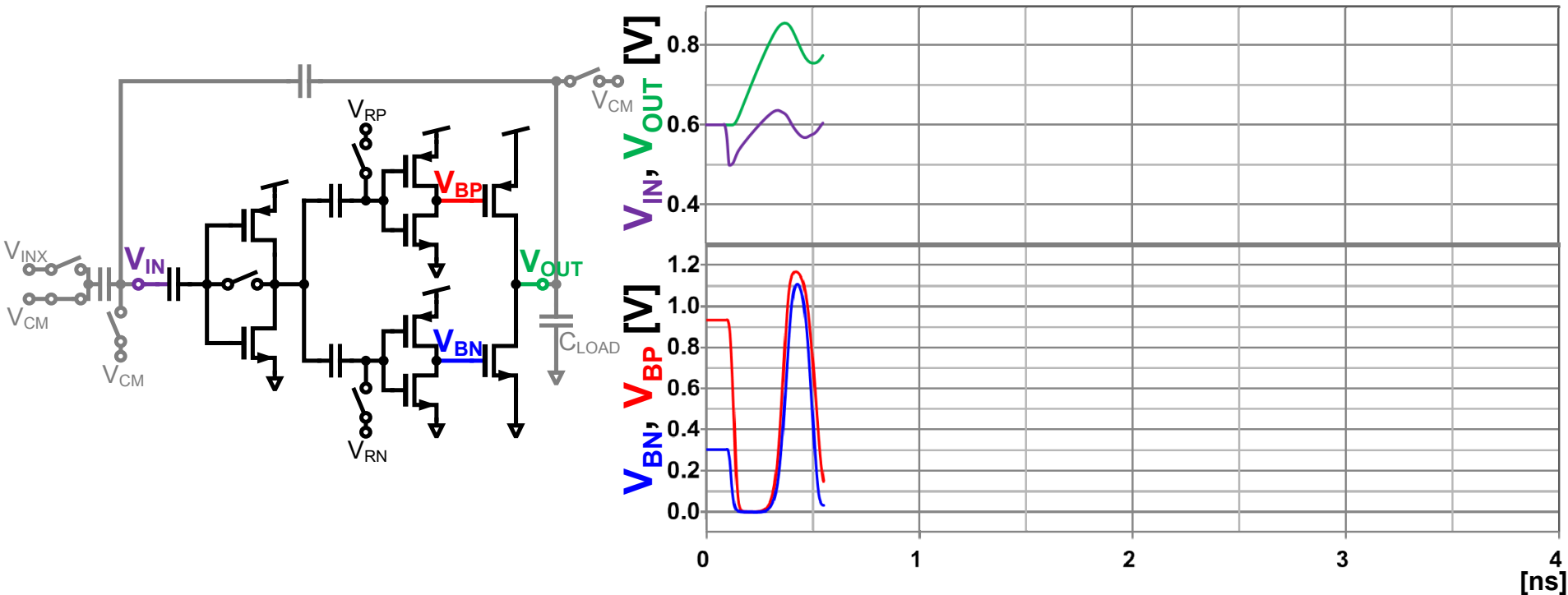
➤ Slew → finite response time → overshoot

Ring Amplifier Large Signal Behavior



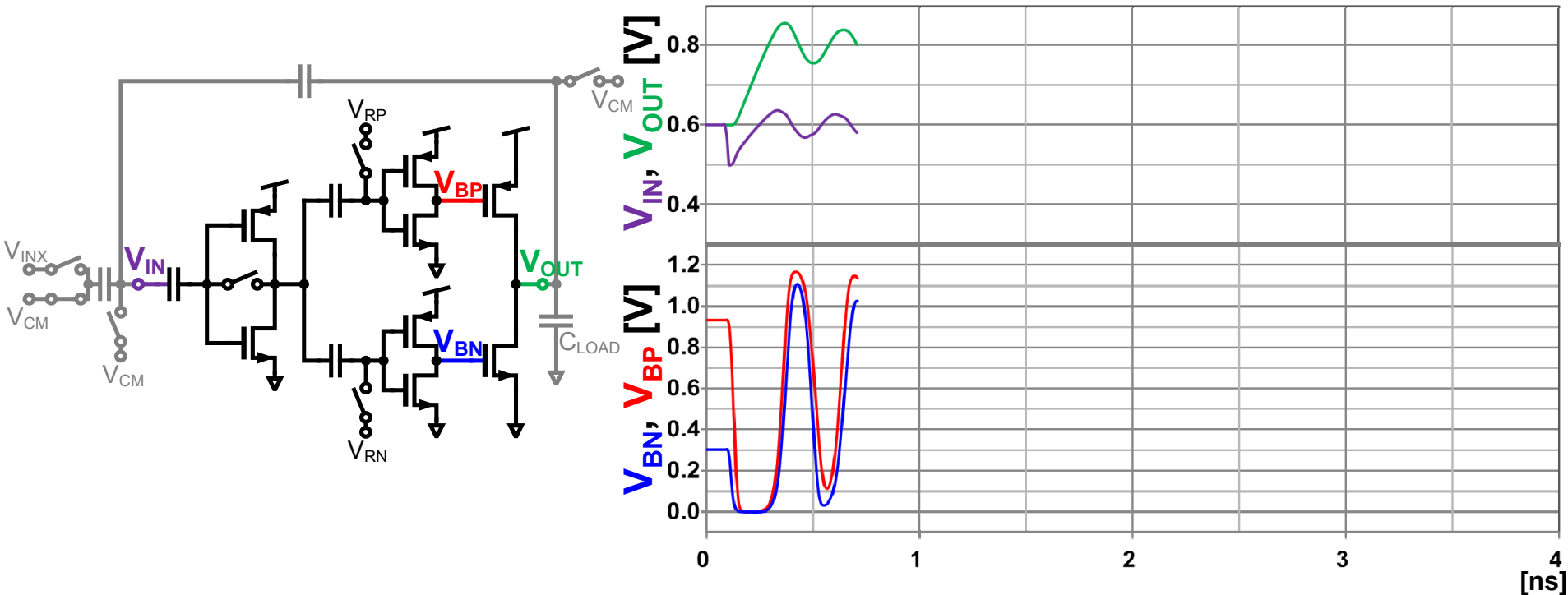
➤ Slew → finite response time → overshoot

Ring Amplifier Large Signal Behavior



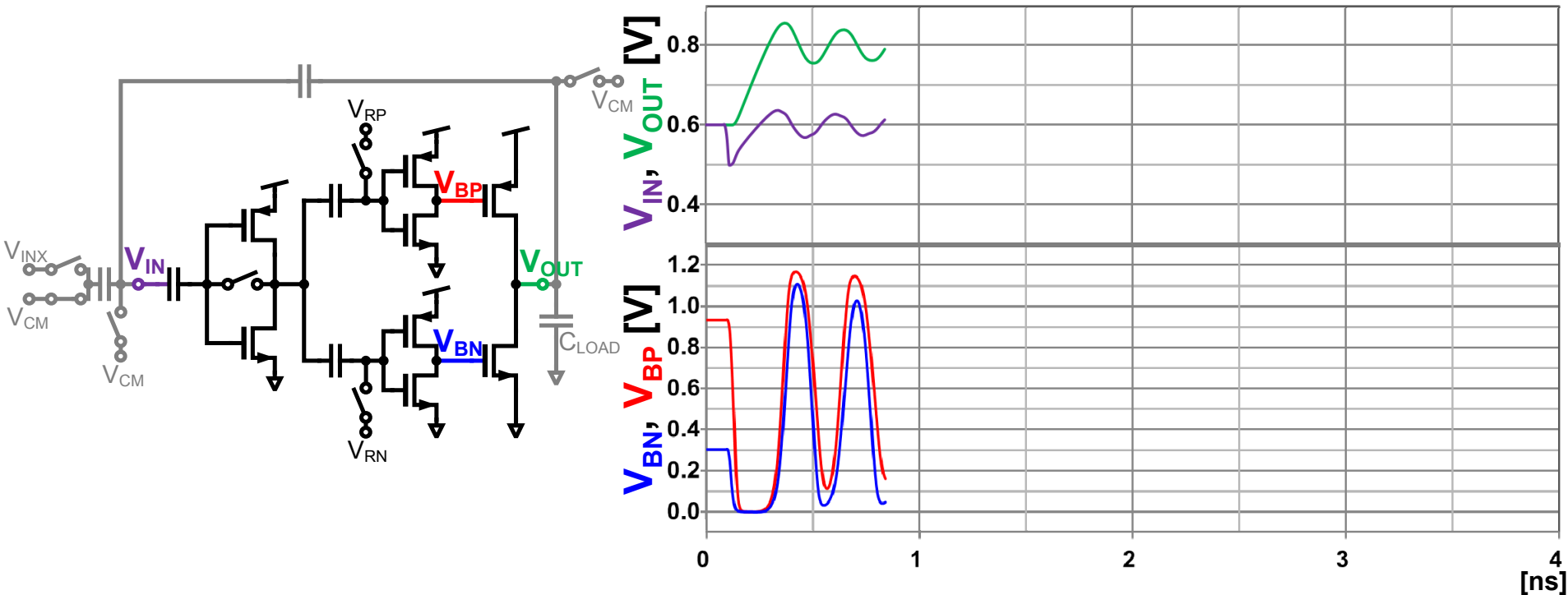
➤ Slew → finite response time → overshoot

Ring Amplifier Large Signal Behavior



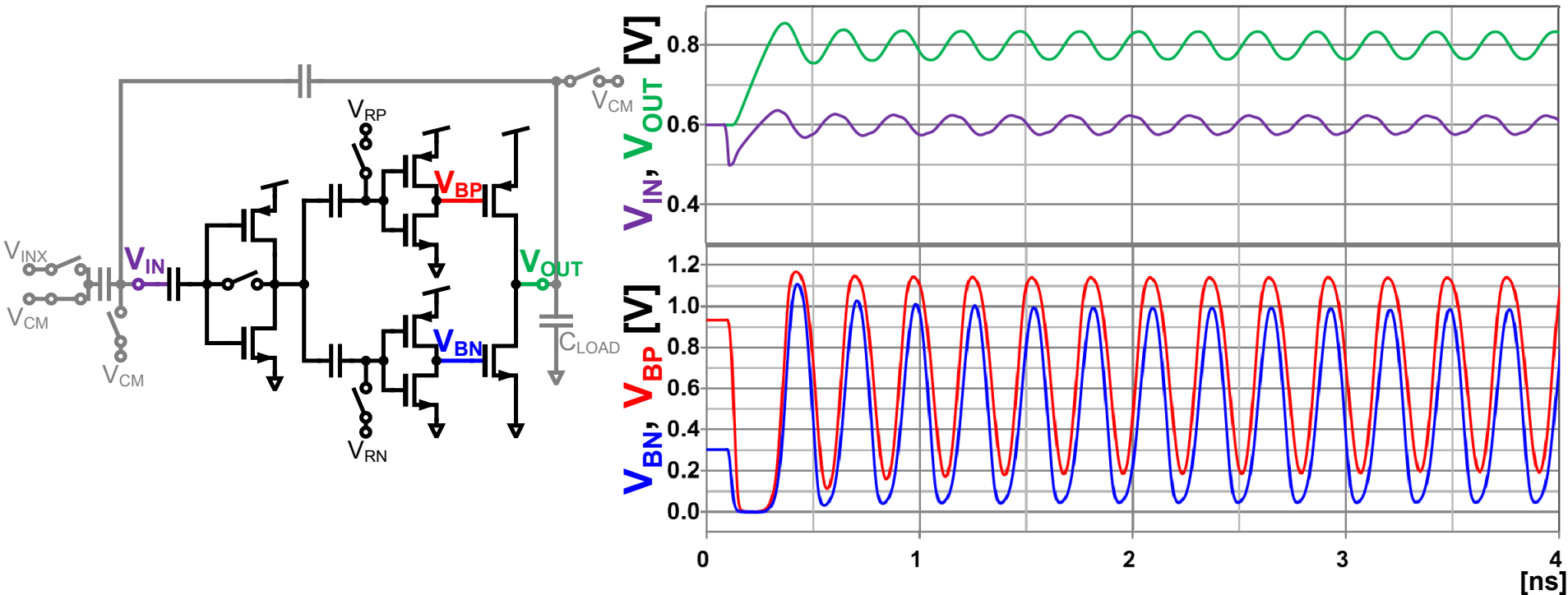
➤ Slew → finite response time → overshoot

Ring Amplifier Large Signal Behavior



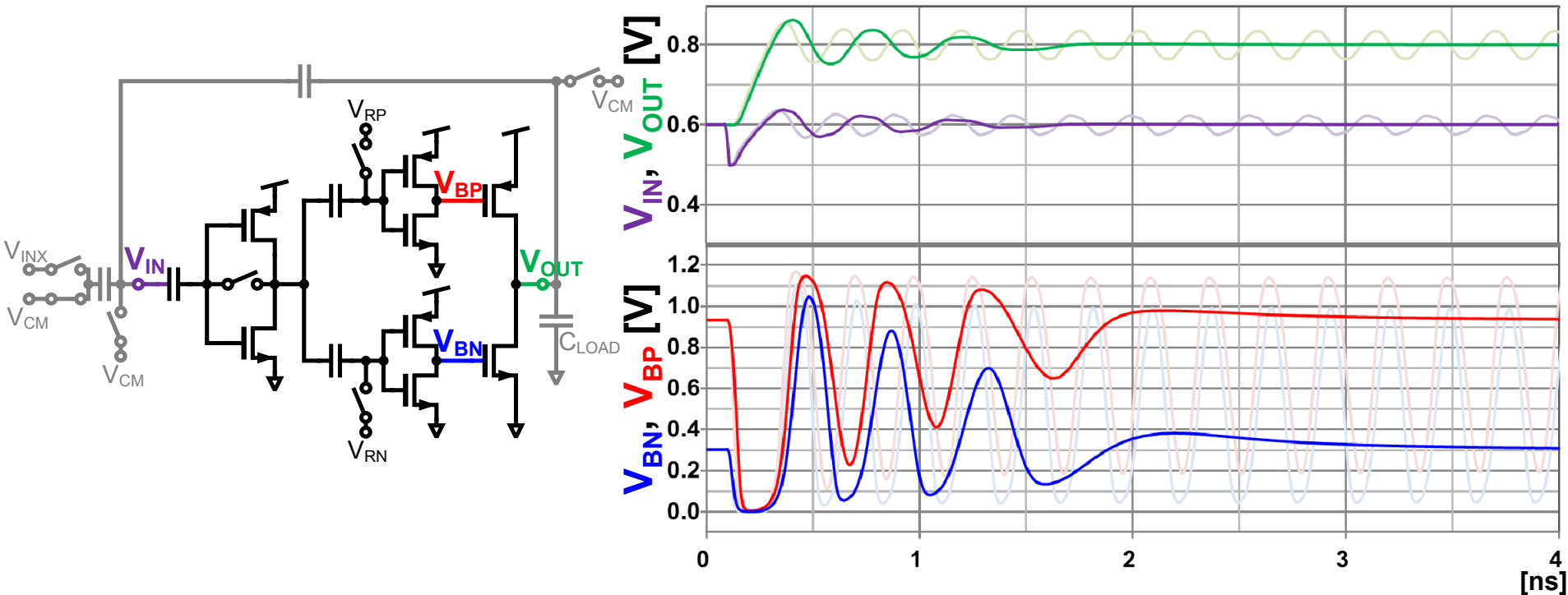
➤ Slew → finite response time → overshoot

Still Oscillates with Positive PM ($=73^\circ$)



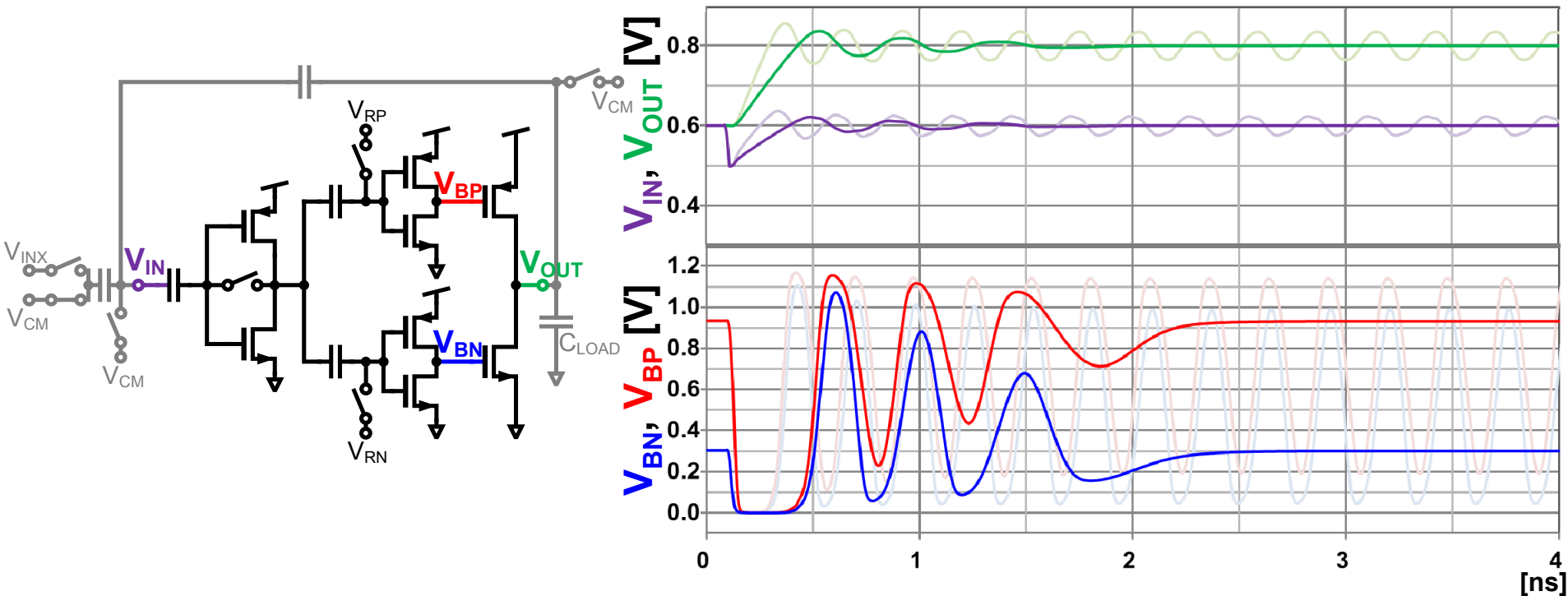
- If overshoot causes the same slew rate as the previous slew
➔ Oscillate!!

Time Domain Stabilization Requirement



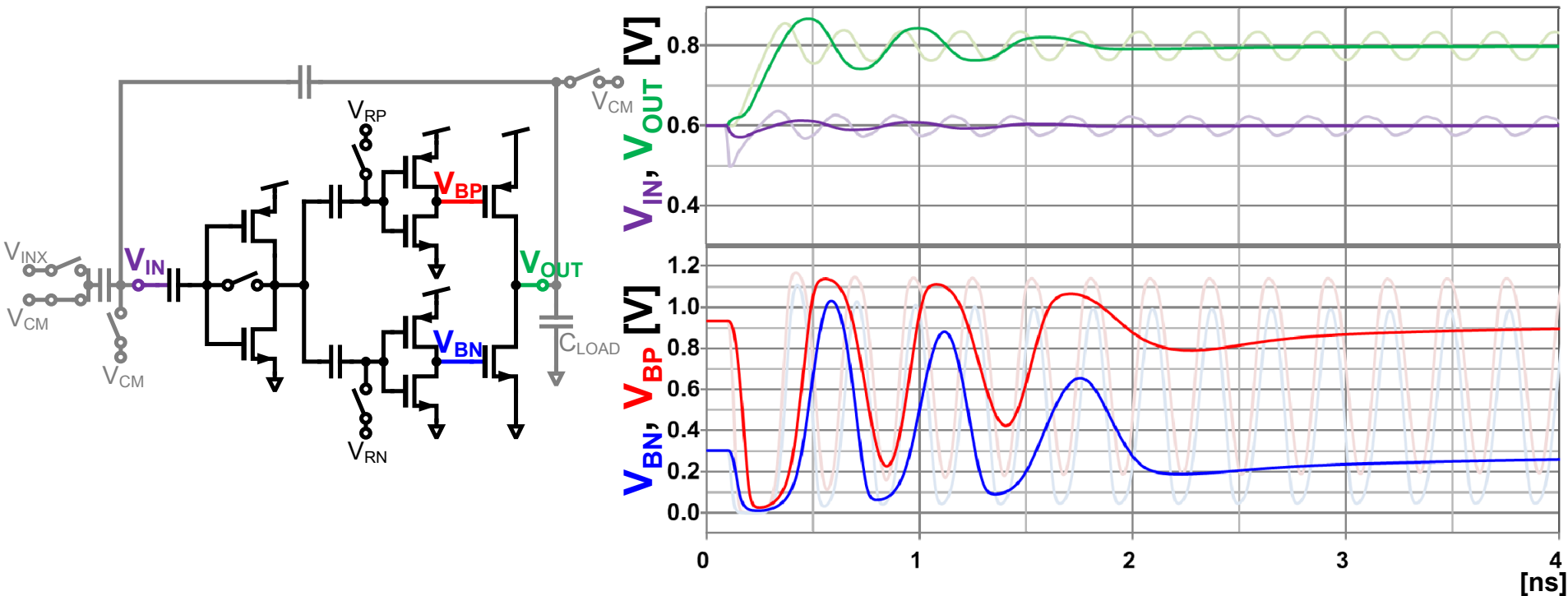
1. V_{BP} , V_{BN} overshoot tuned to decrease each successive oscillation (by gain \downarrow)

Time Domain Stabilization Requirement



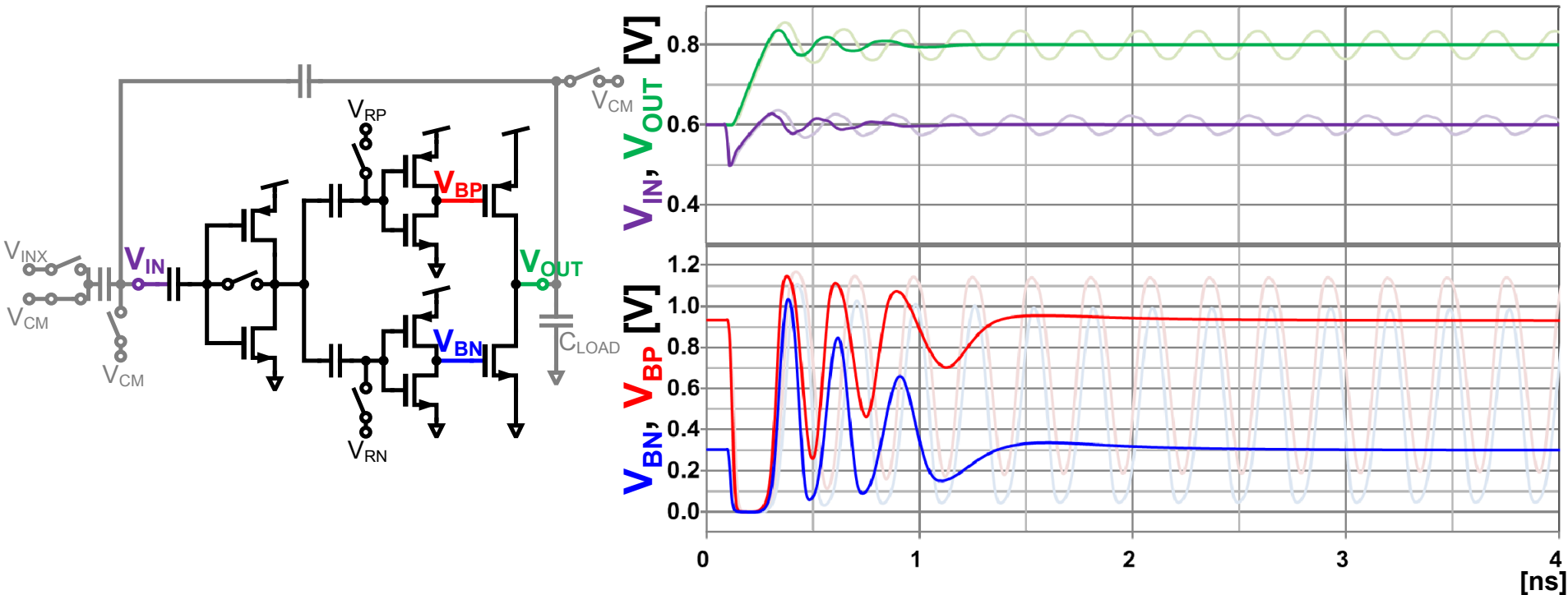
2. V_{BP} , V_{BN} overshoot tuned to decrease each successive oscillation (by slew ↓)

Time Domain Stabilization Requirement



3. V_{BP} , V_{BN} overshoot tuned to decrease each successive oscillation (by feedback factor ↓)

Time Domain Stabilization Requirement

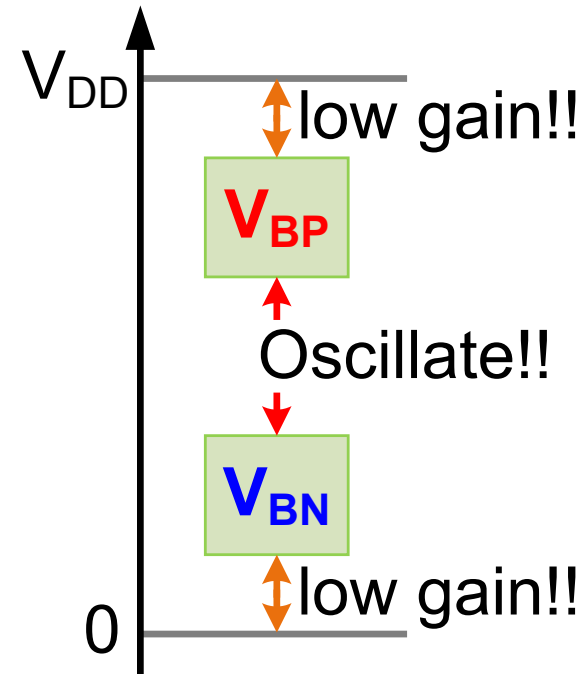
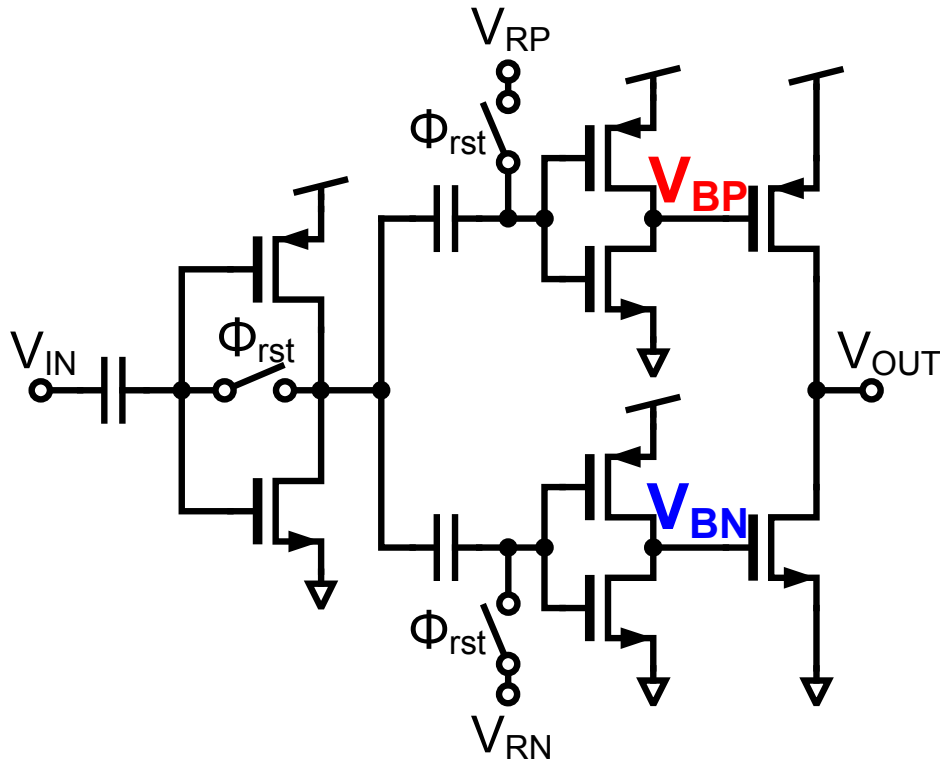


4. V_{BP} , V_{BN} overshoot tuned to decrease each successive oscillation (by 1st, 2nd inv. BW \uparrow)
→ Slew & overshoot gradually decrease → stabilized

Ring Amplifier Advantages

- 😊 High efficiency slew-based charging
- 😊 Almost rail-to-rail output
- 😊 60~70dB gain from 3 inverter stages

Ring Amplifier Disadvantages

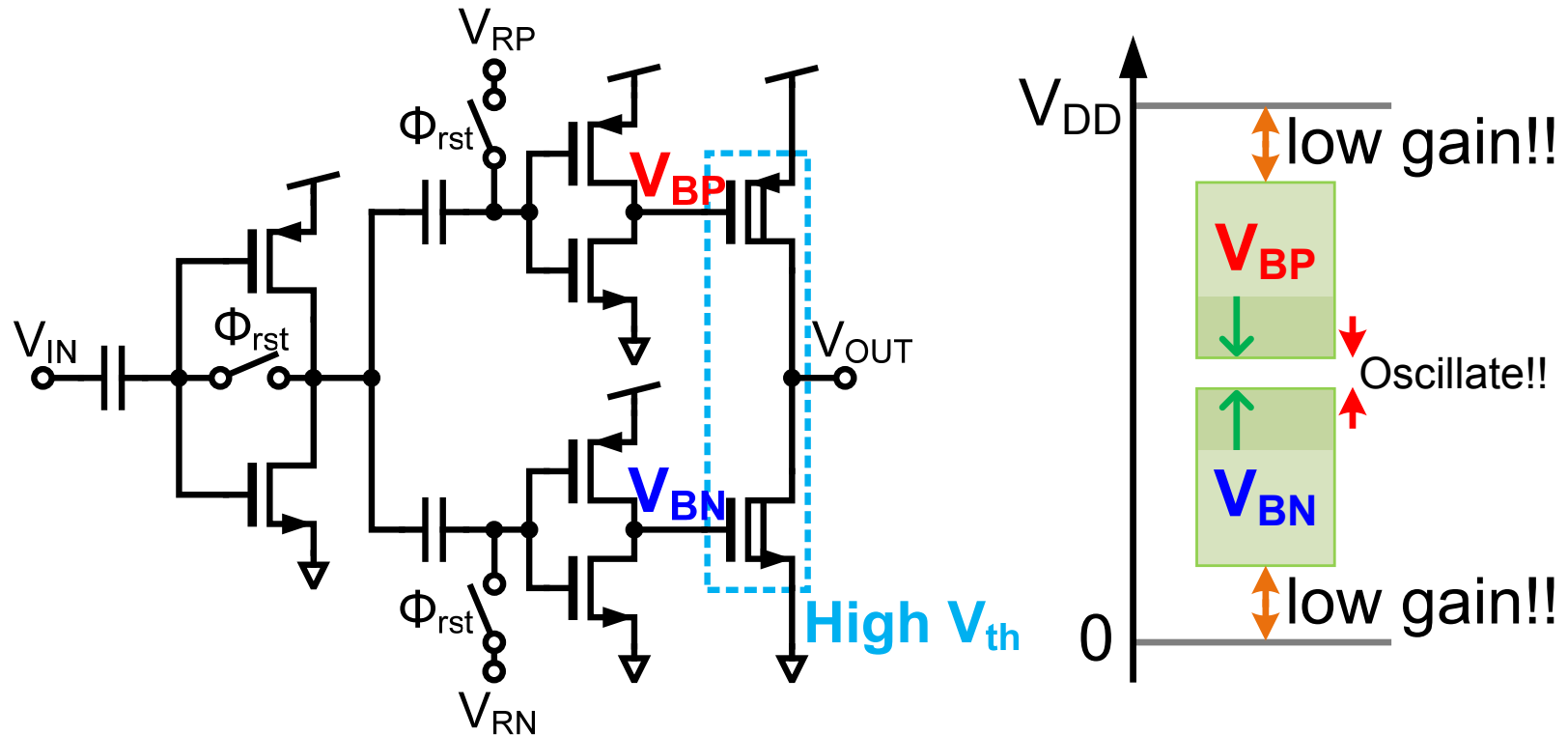


☹️ Narrow offset voltage range sweet spot

- Output common mode follows $(V_{RN} + V_{RP})/2$
- Sensitive to V_{th} variation

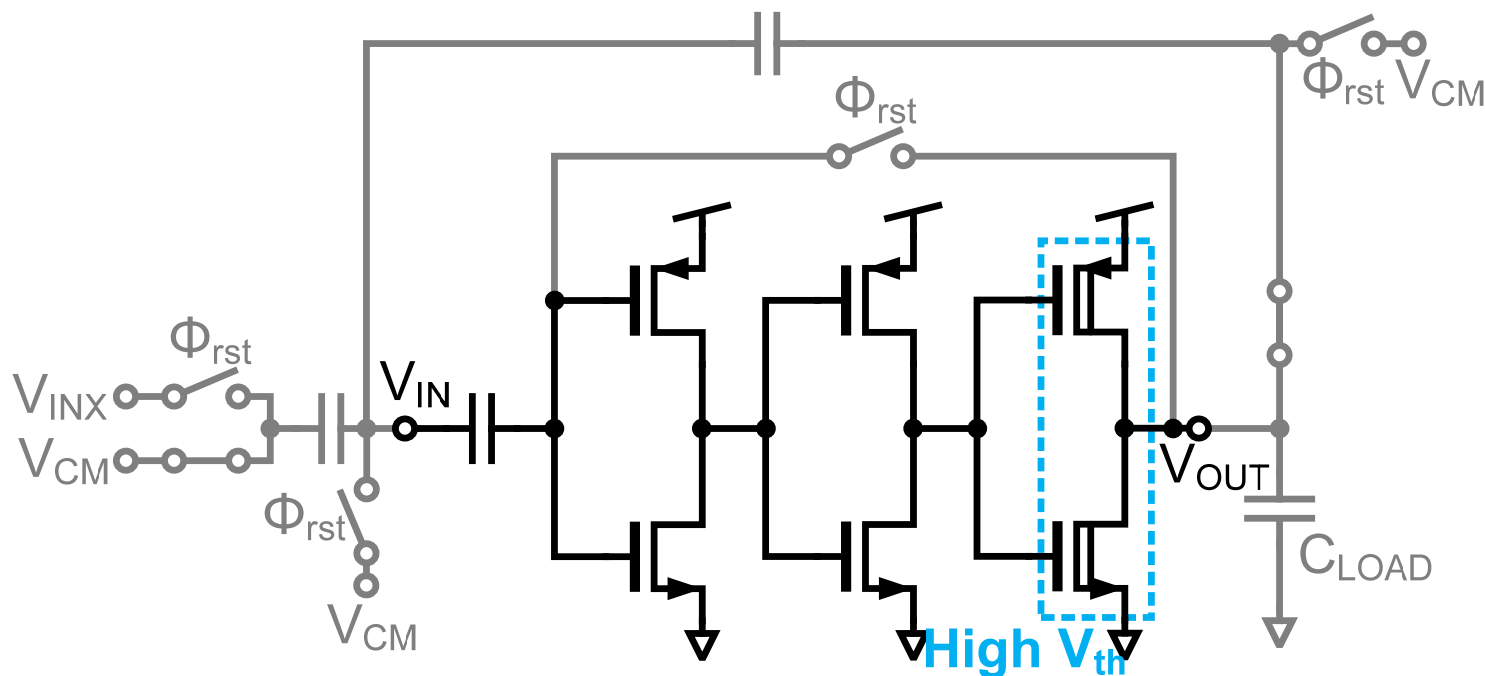
Self-biased Ring Amplifier

High Threshold Voltage 3rd Inverter



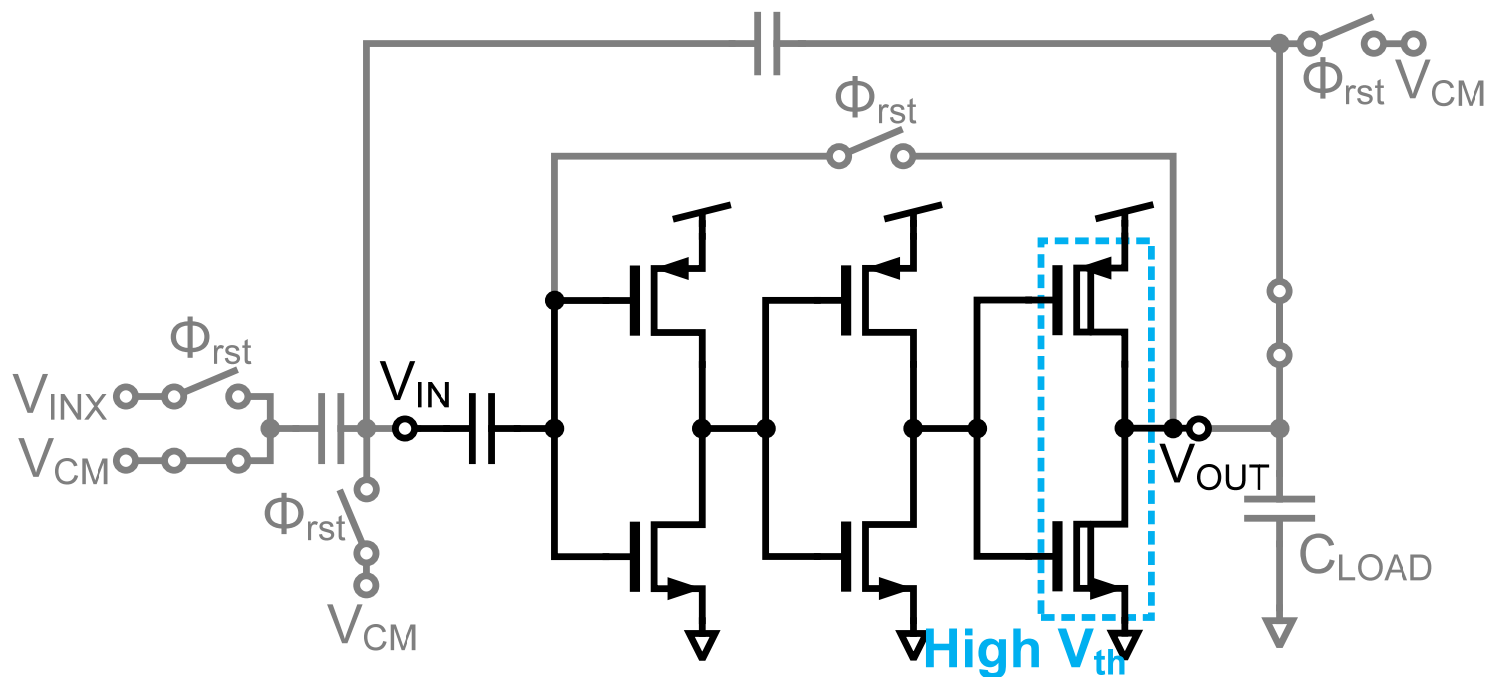
- Order of magnitude higher output resistance for the same offset
 - ➔ Extend offset range

Ring Amplifier without Offset



- When $V_{th:N} + |V_{th:P}| > V_{DD}$
- Remove 2nd stage split, offset capacitors
 - ➔ Power reduction
 - ➔ Auto-zero → stable output common mode

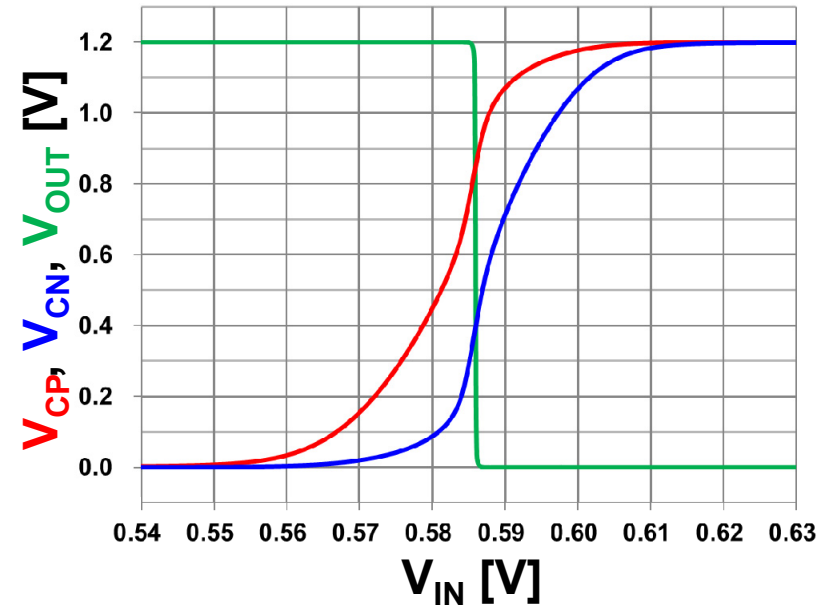
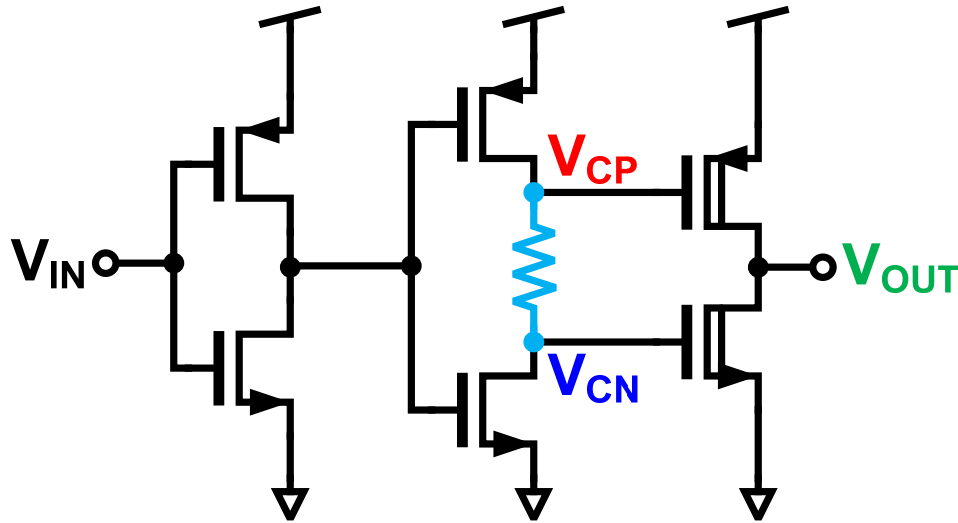
Ring Amplifier without Offset



☹ $V_{th:N} + |V_{th:P}| > V_{DD} \rightarrow$ **not always true**

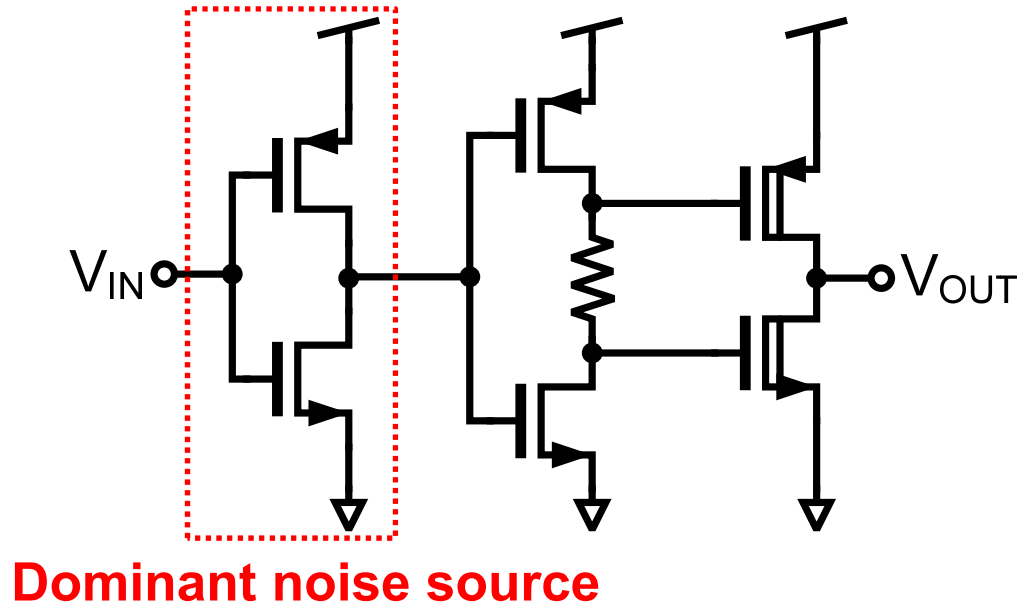
➤ **Still require offsets, but w/o external bias??**

Applying Offset using Resistor



- Dynamically apply offset using IR drop
- Offset tracks V_{DD}

Noise and Power Optimization

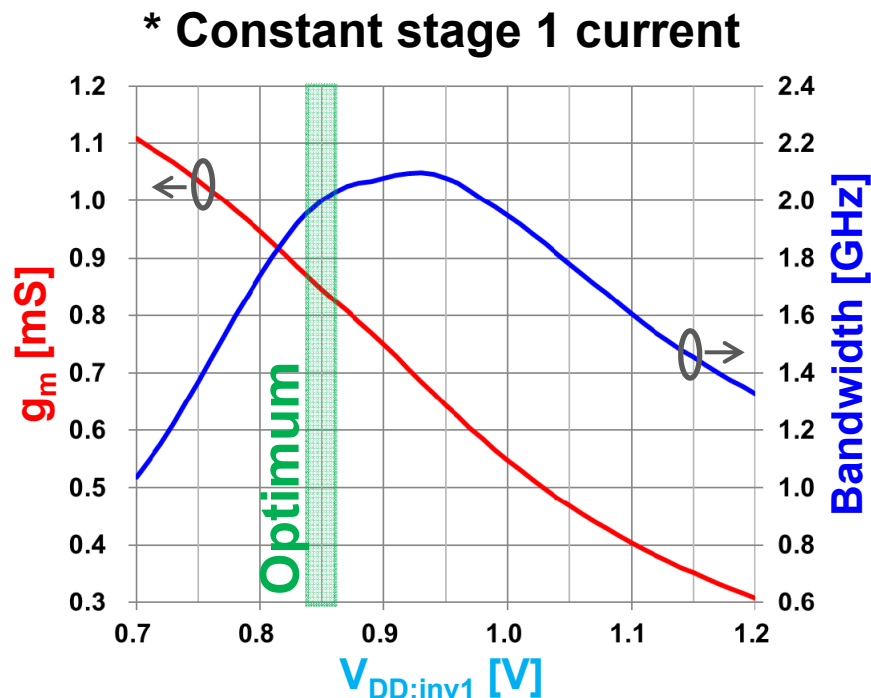
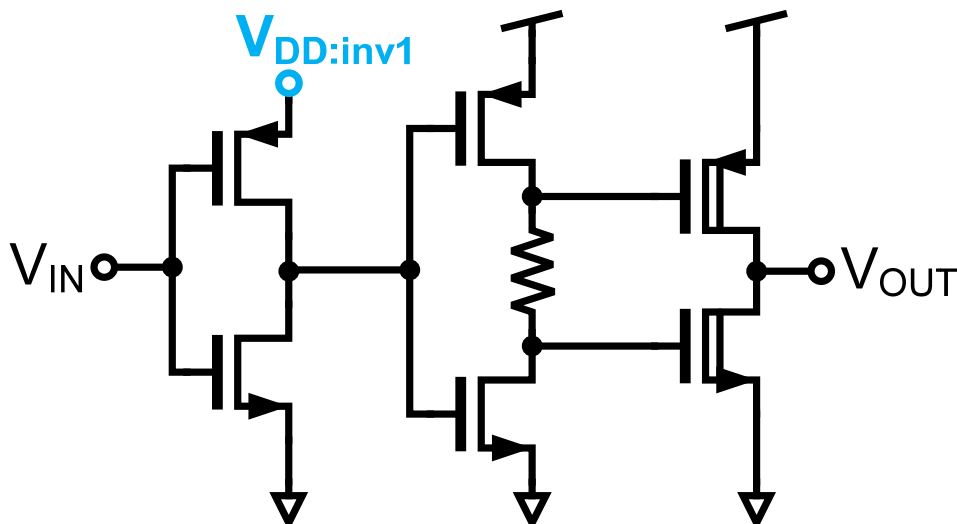


➤ Noise & power trade off

- Inv. thermal noise $\propto 1/g_m$

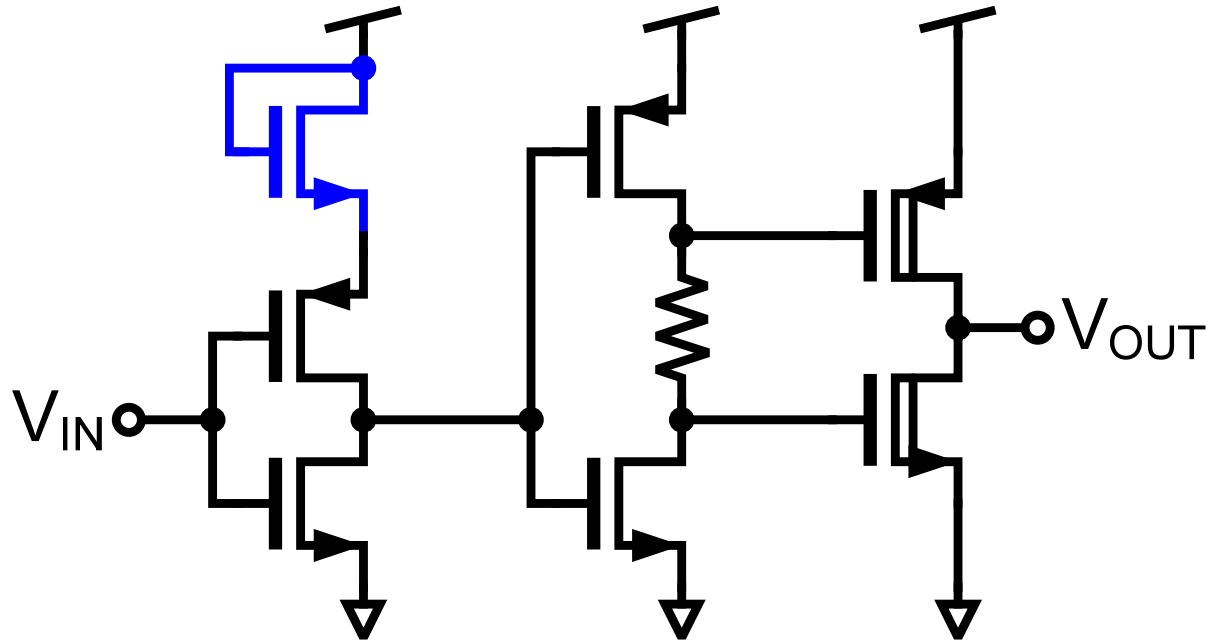
Noise $\downarrow \rightarrow g_m \uparrow \rightarrow W \uparrow \rightarrow \text{power} \uparrow$

Optimum First Stage V_{DD} ($V_{DD:inv1}$)



- Better g_m/I_D when $V_{DD:inv1} \downarrow$
- Optimum g_m , bandwidth with lower $V_{DD:inv1}$

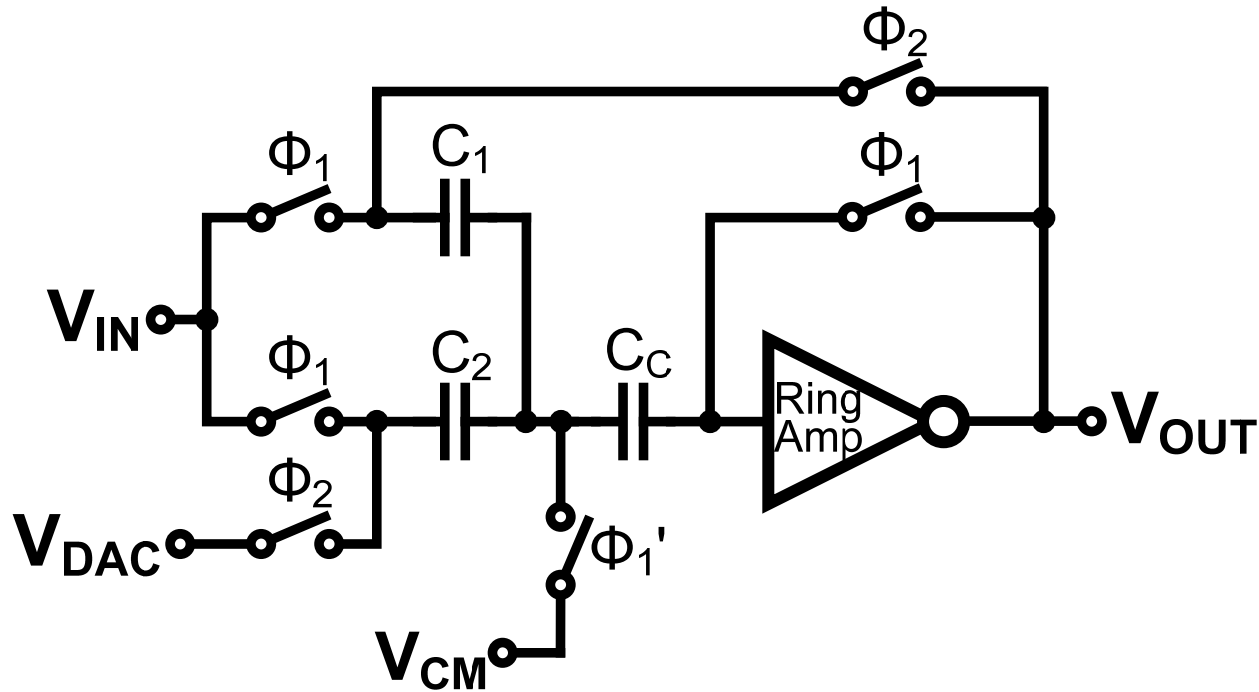
NMOS Diode as Internal Regulator



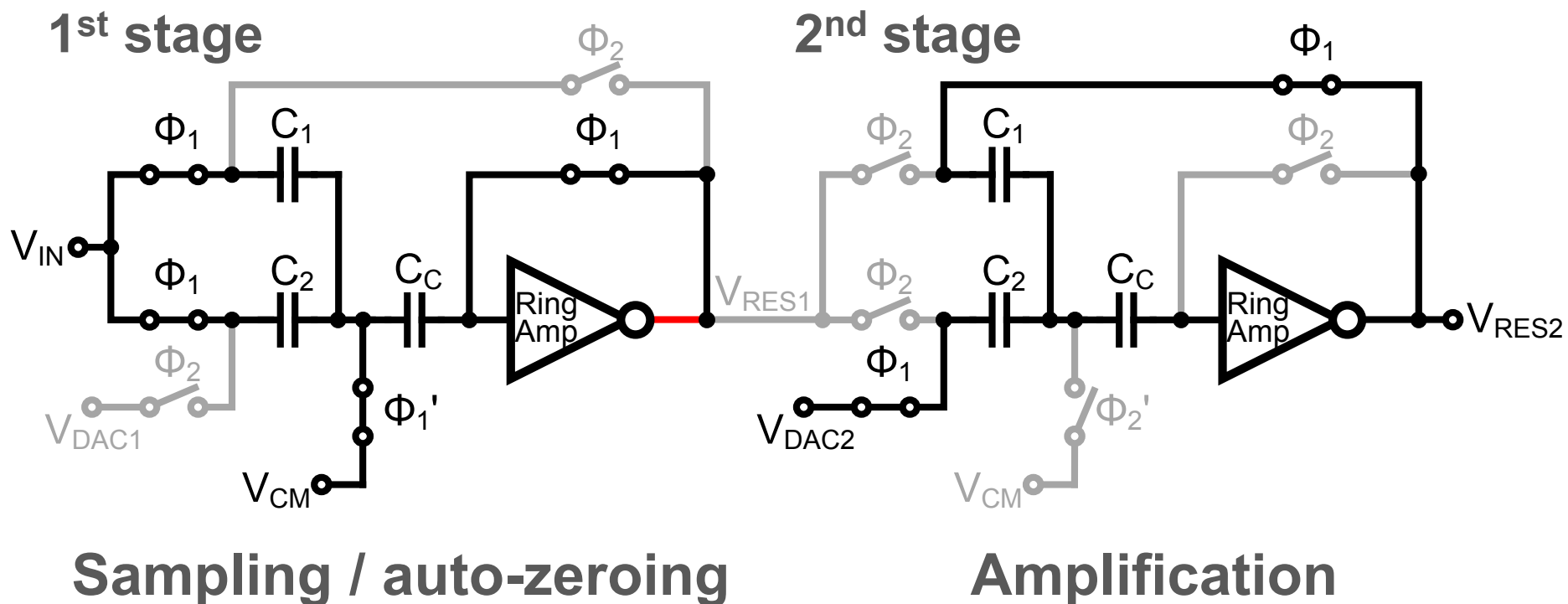
Auto-zeroed Ring Amplifier MDAC

- 1) Stabilize auto-zero**
- 2) Eliminate auto-zero switch cap gain error**

Auto-zeroed Flip-around MDAC

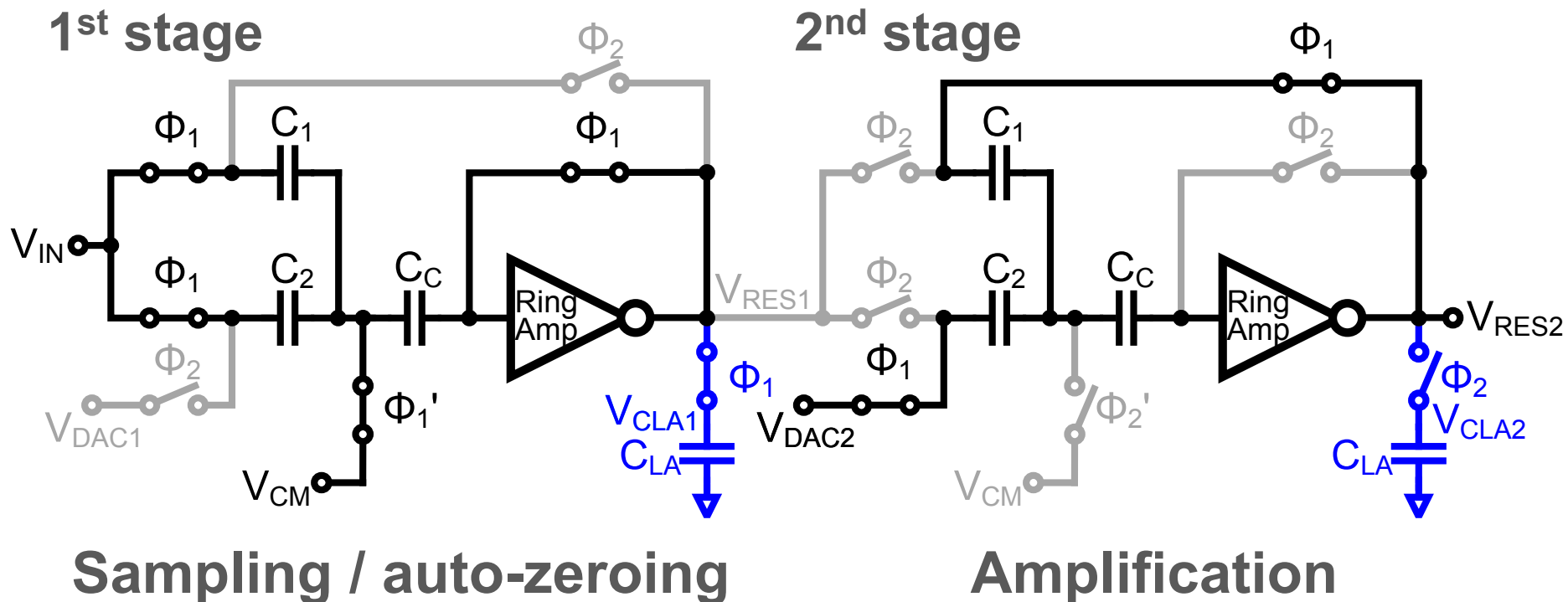


Small Load During Auto-zeroing



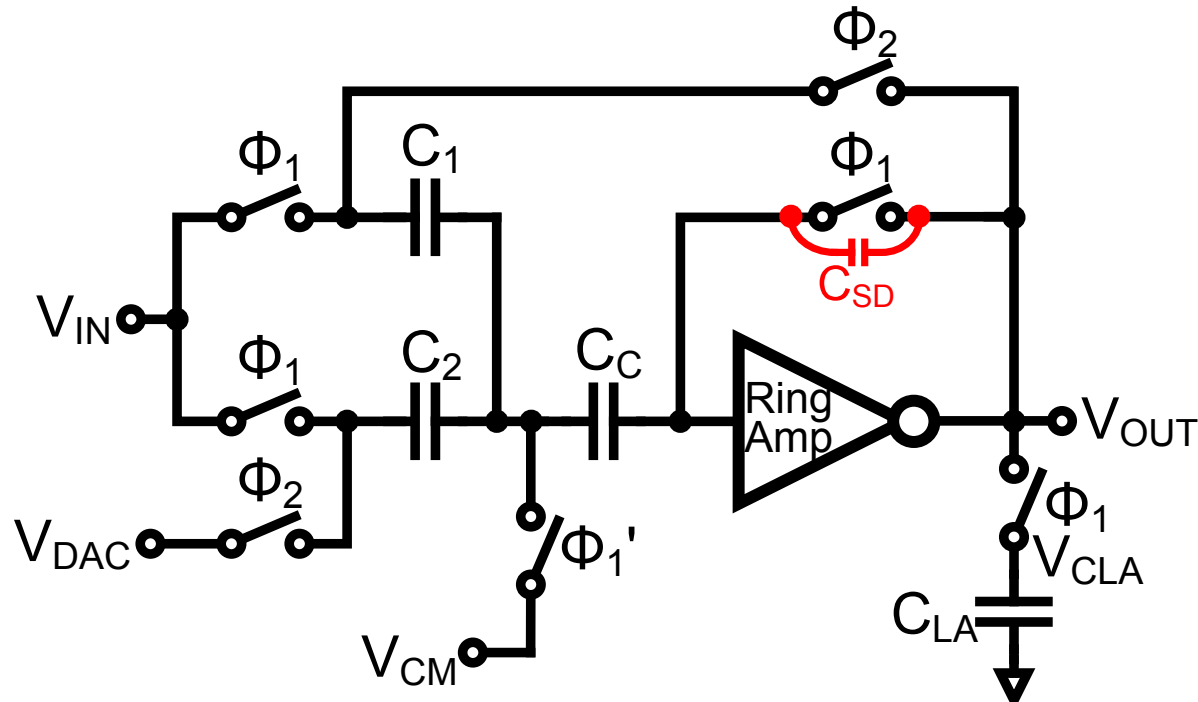
☹ Small $C_L \rightarrow$ Oscillate!!

Additional Loading During Auto-zero



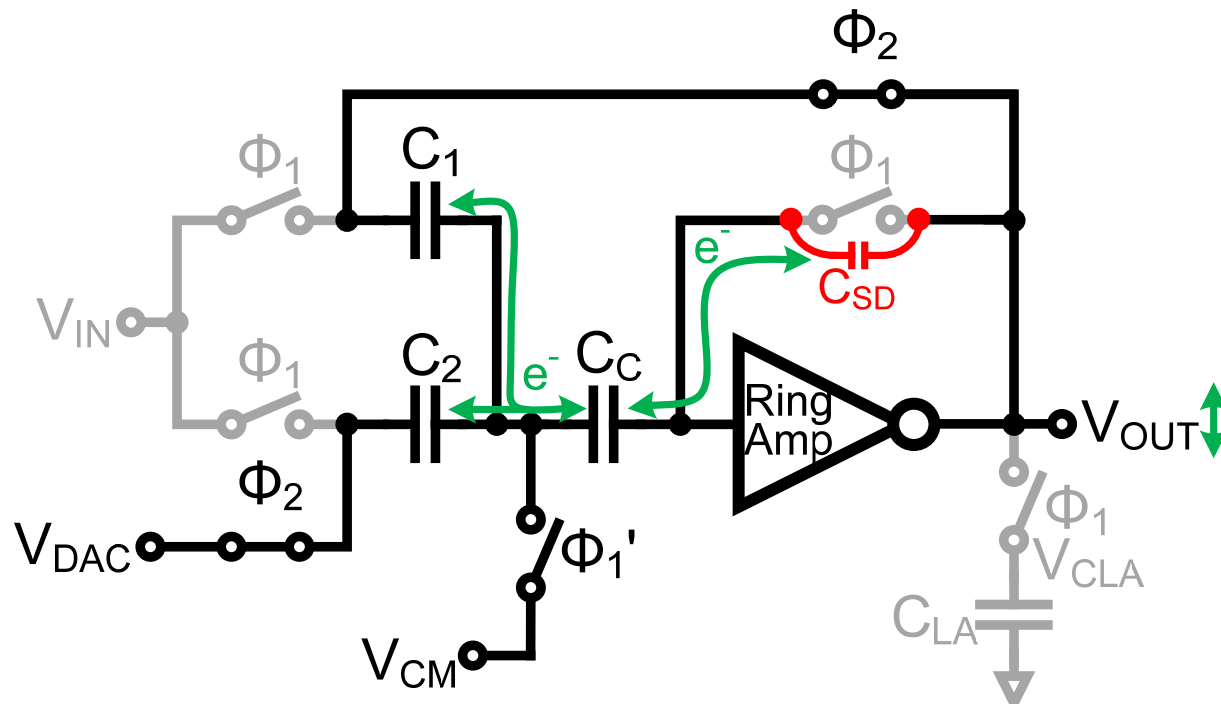
- Unity gain feedback $\Rightarrow C_{LA} > 2(C_1 + C_2)$
- V_{CLA} stays constant \Rightarrow no additional power

Auto-zero Switch C_{SD} Problem

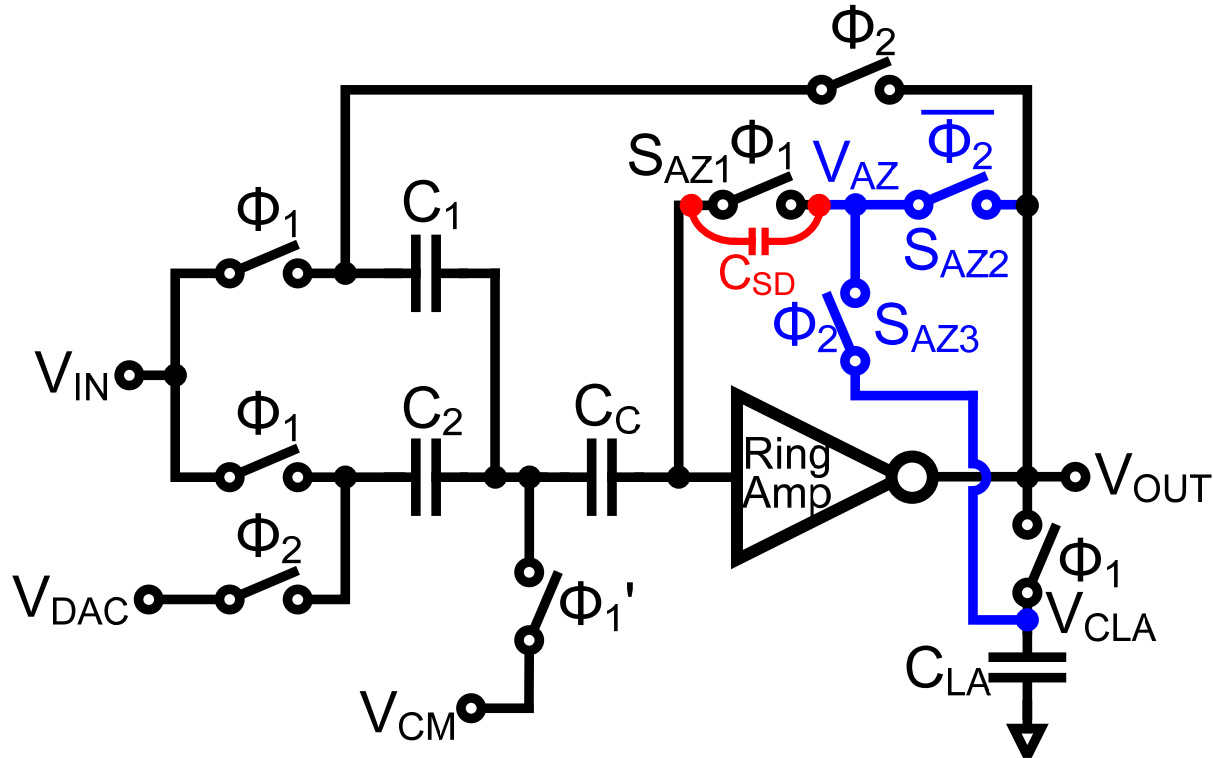


➤ Switch S to D parasitic capacitor

Gain Error Due to C_{SD}

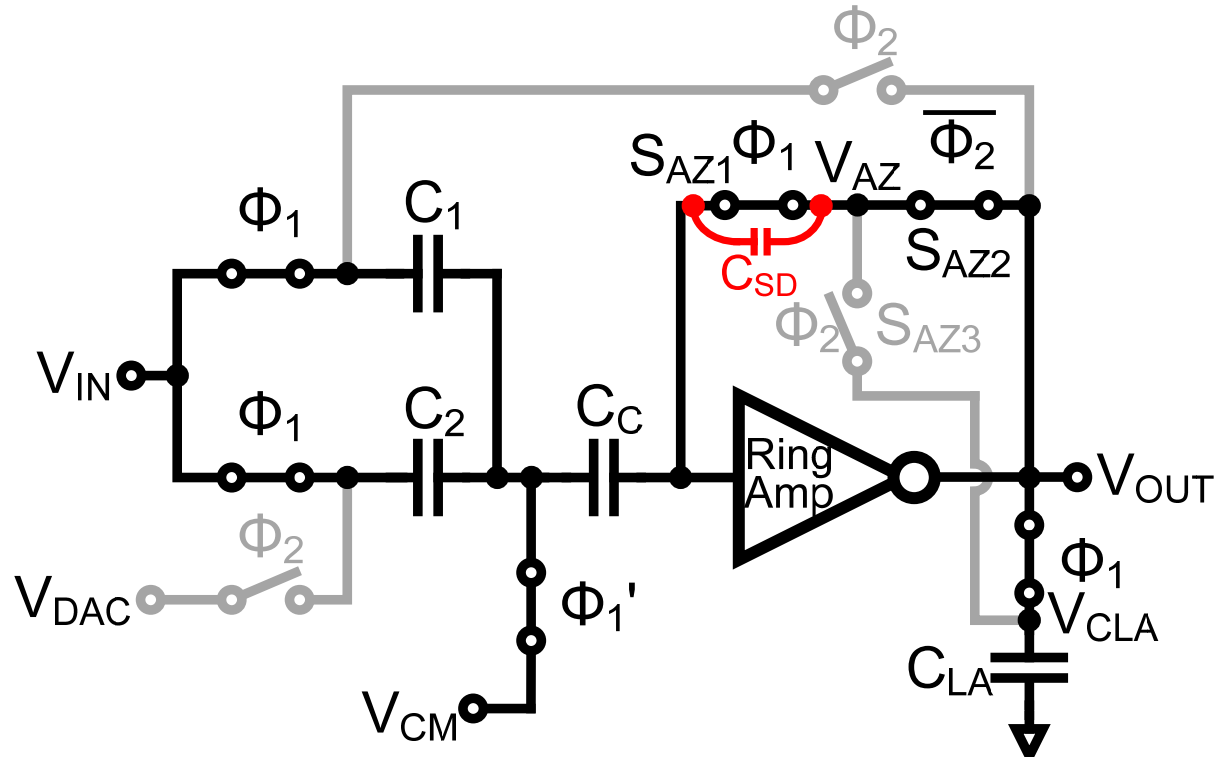


Improved Auto-zero Switch



➤ Eliminate C_{SD} caused gain error

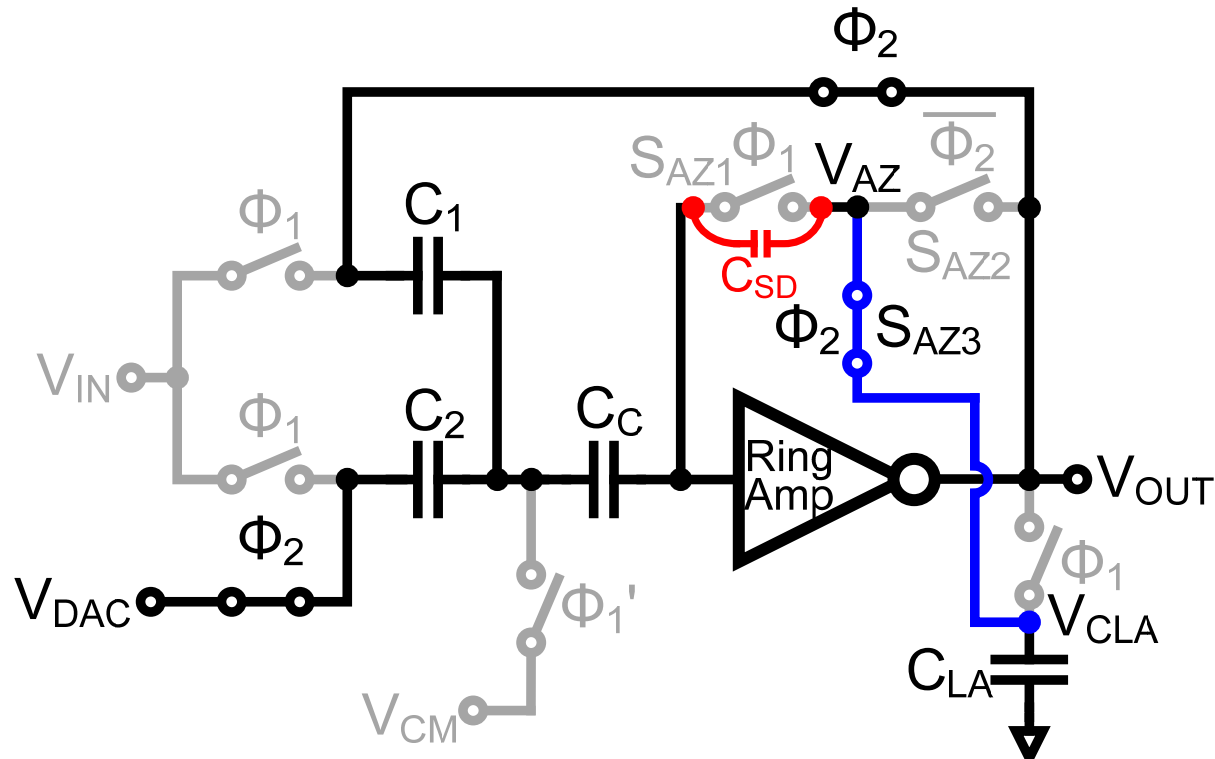
Improved Auto-zero Switch



➤ Auto-zero phase

- Same as conventional auto-zero

Improved Auto-zero Switch

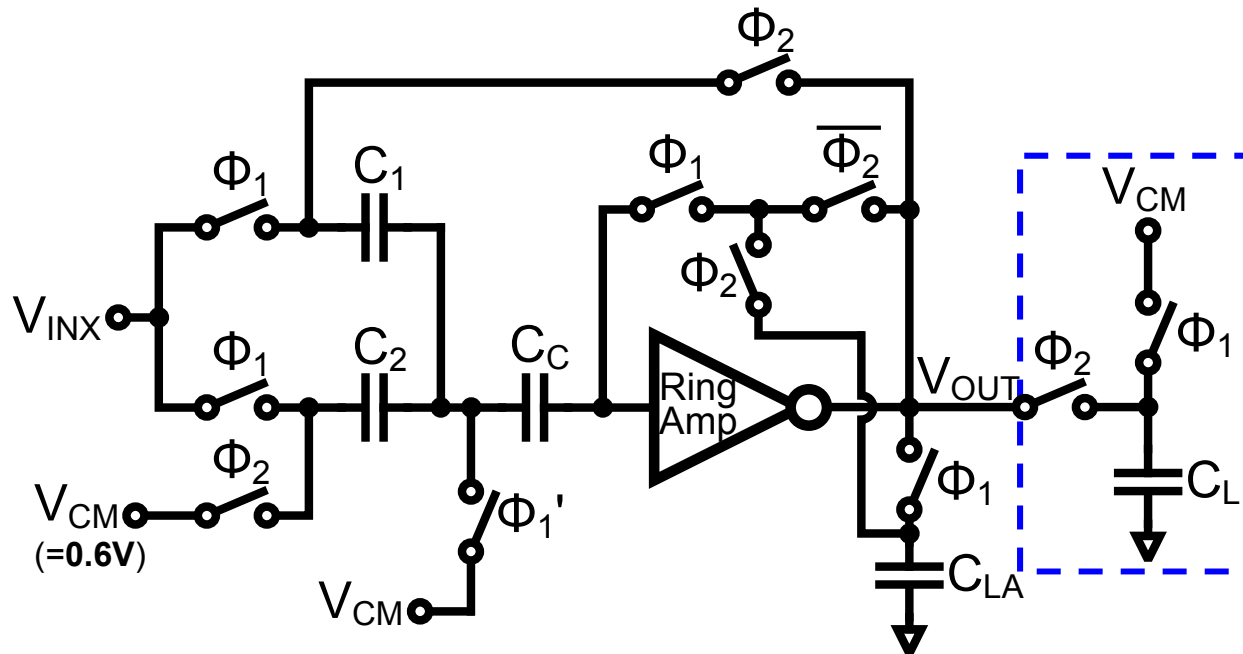


➤ Amplification phase

- Effectively grounding C_{SD}
- ➔ Eliminates C_{SD} related gain error

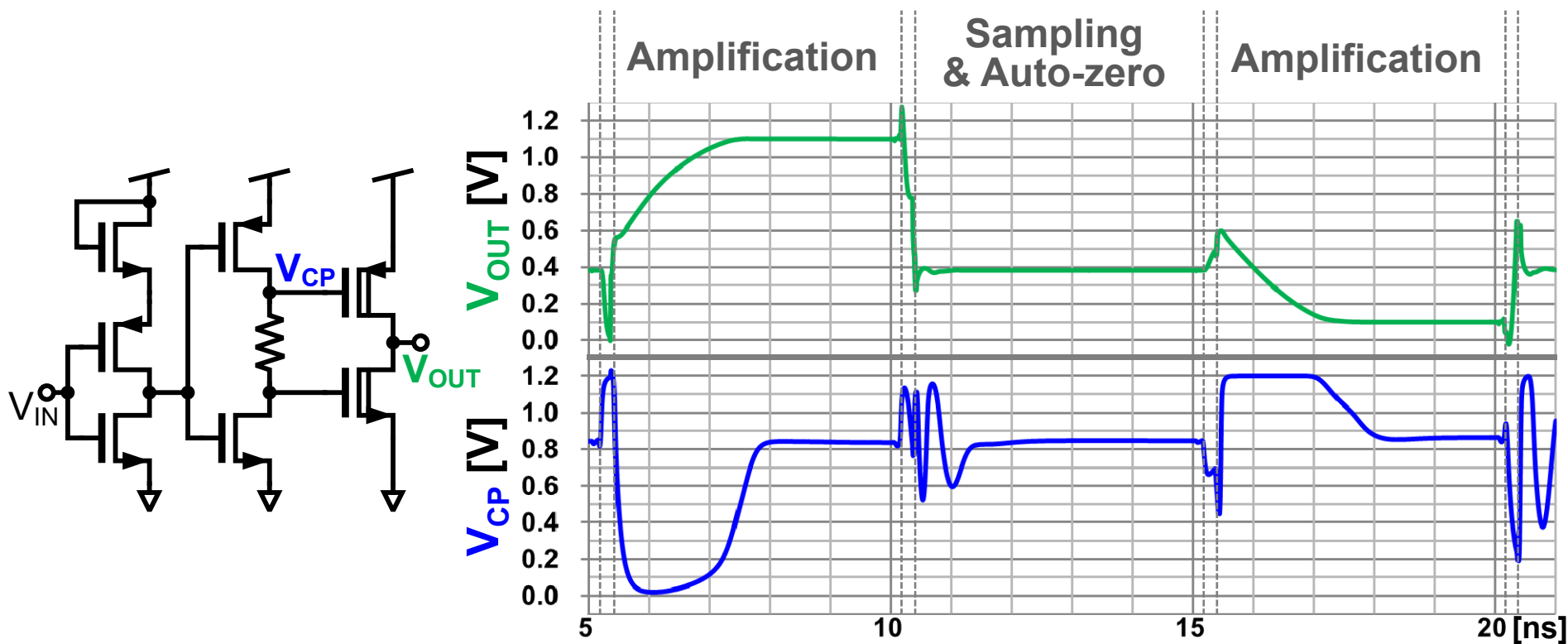
Comparator-less Sub-ADC

Ring Amplifier Operation in MDAC



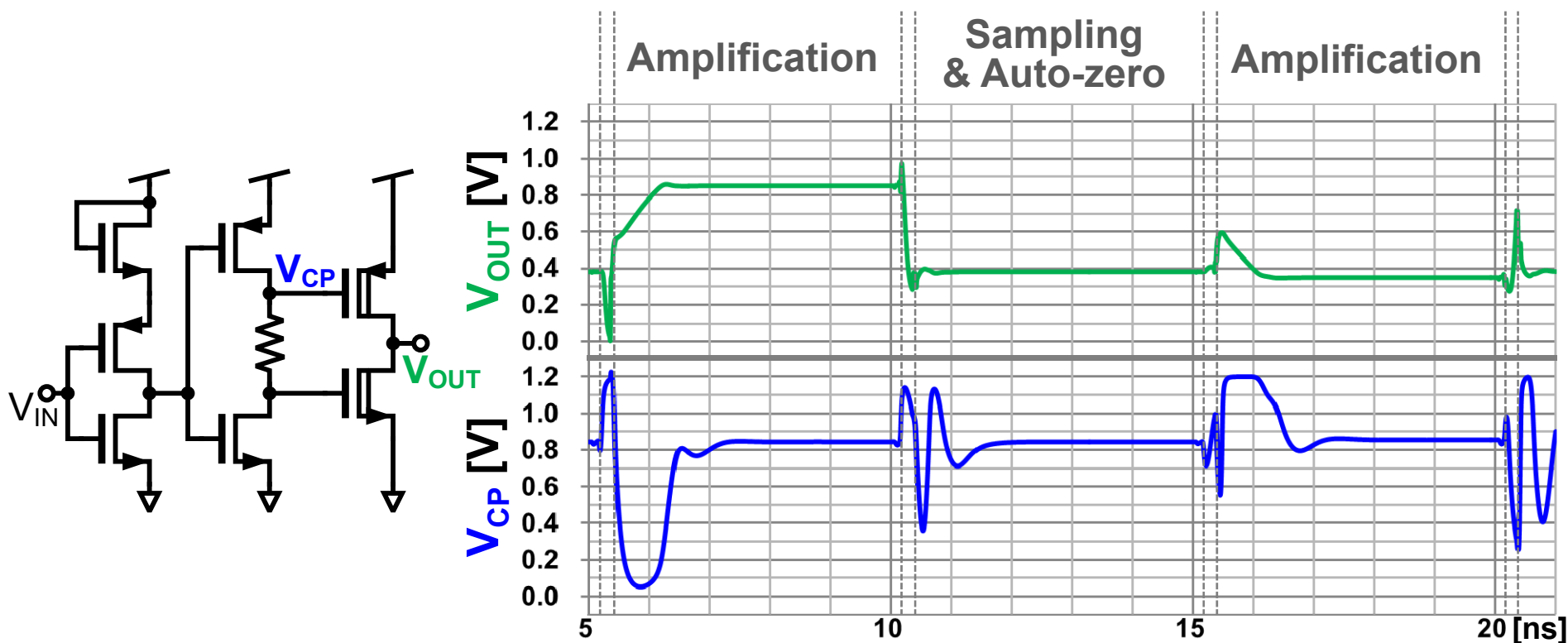
- **Ring amp operation in amplification phase**
 - Reset load to V_{CM} before amplification

Ring Amplifier Operation in MDAC



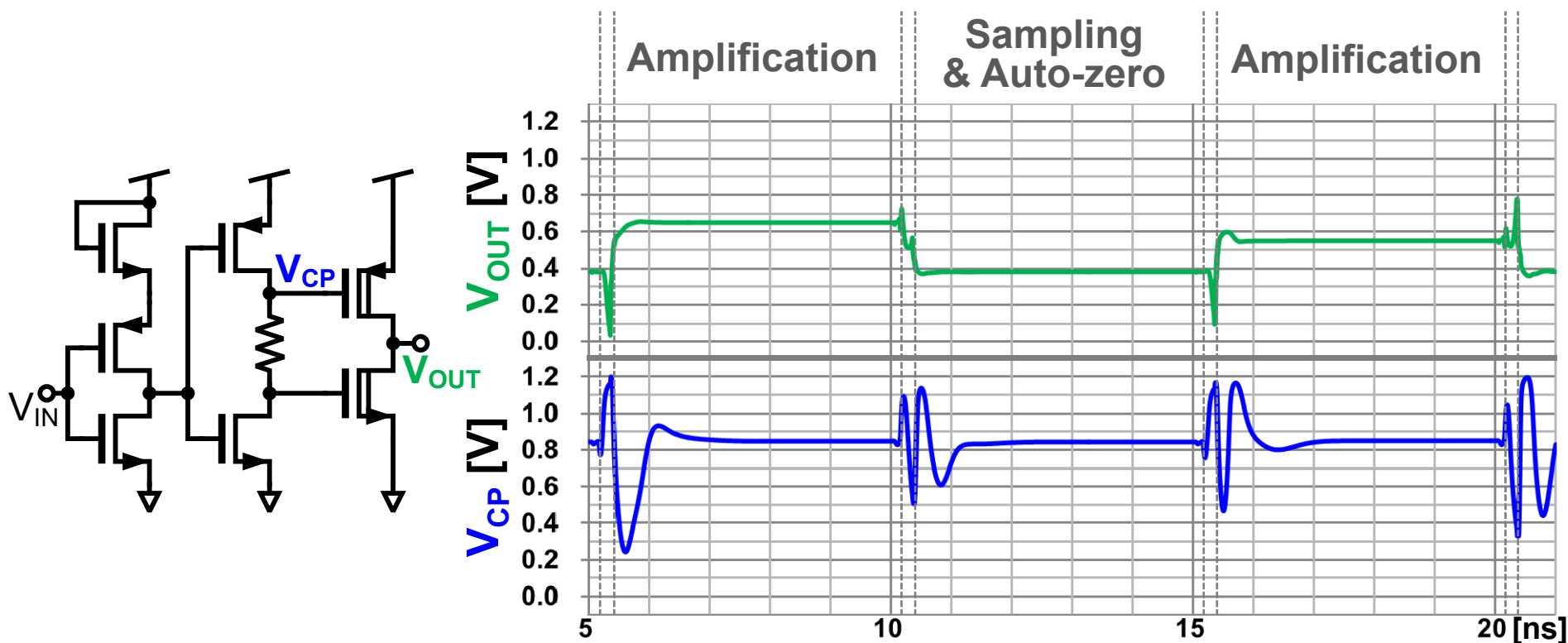
➤ Square wave input $V_{INX:pk-pk} = 500mV$

Ring Amplifier Operation in MDAC



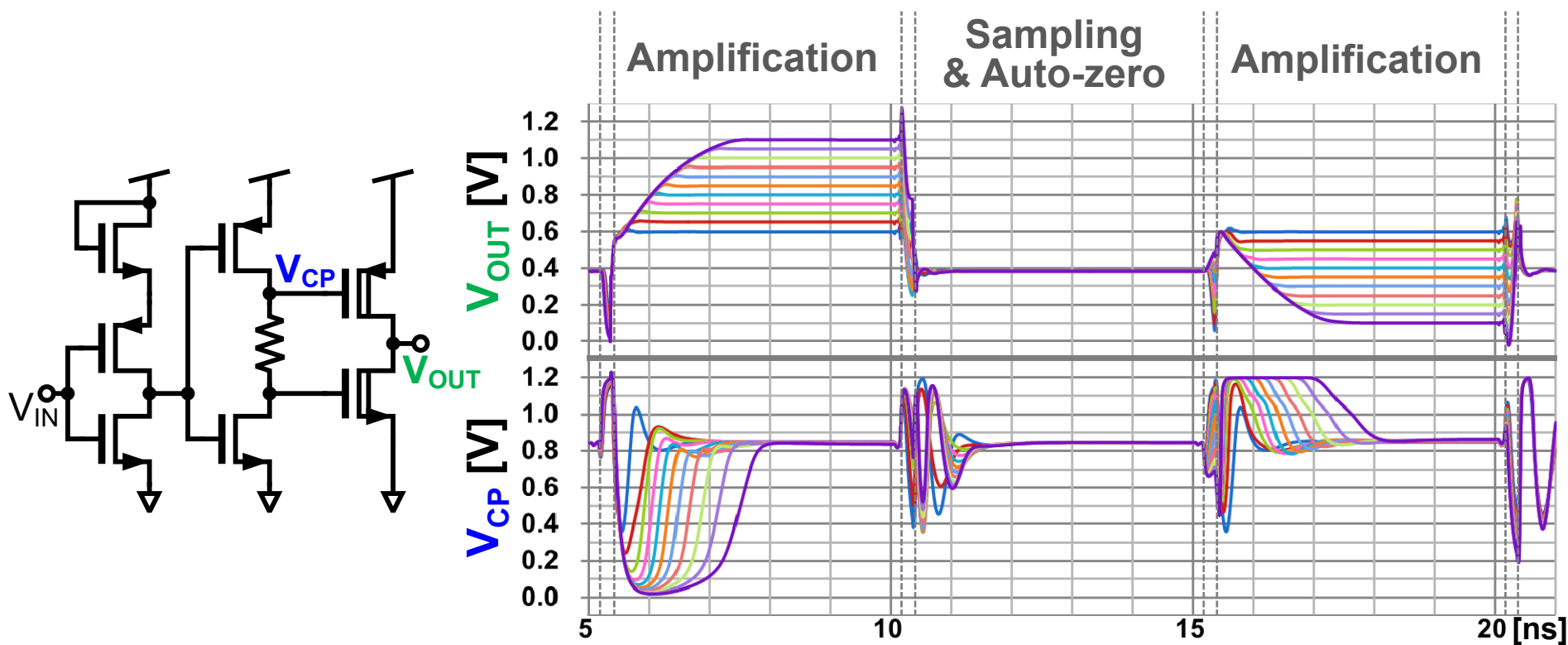
➤ Square wave input $V_{INX:pk-pk} = 250mV$

Ring Amplifier Operation in MDAC



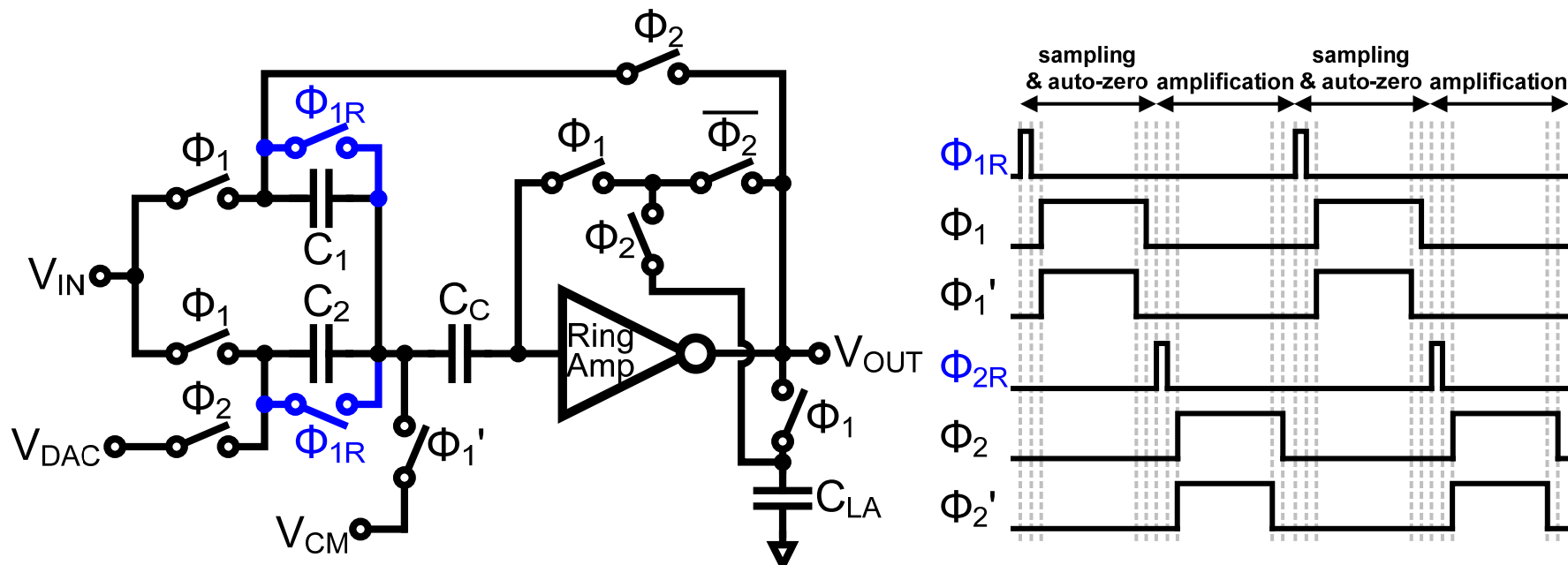
➤ Square wave input $V_{INX:pk-pk} = 50\text{mV}$

Ring Amplifier Operation in MDAC



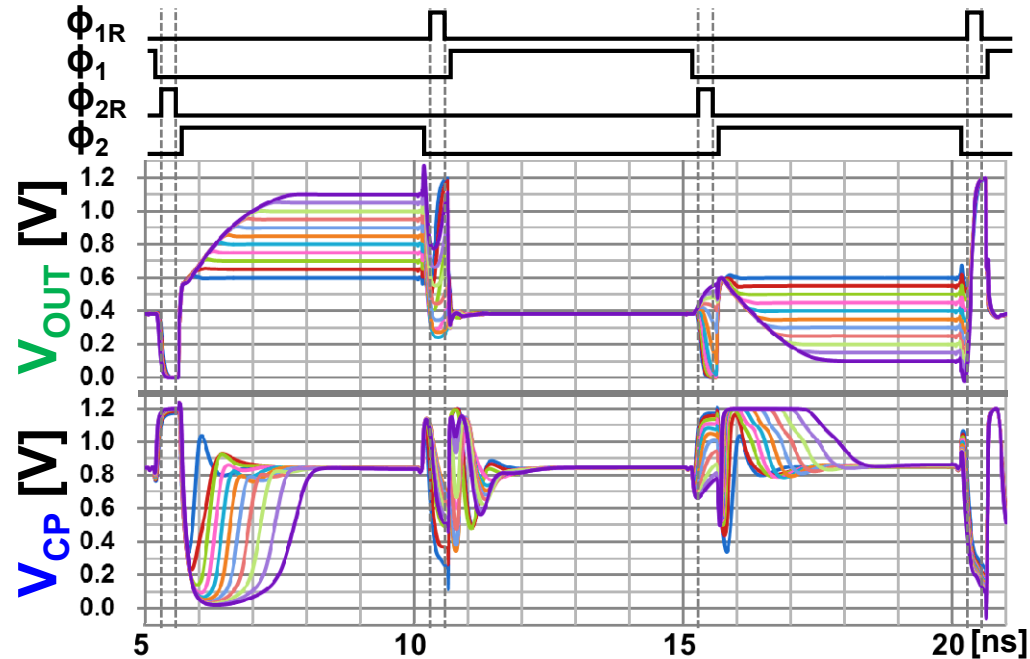
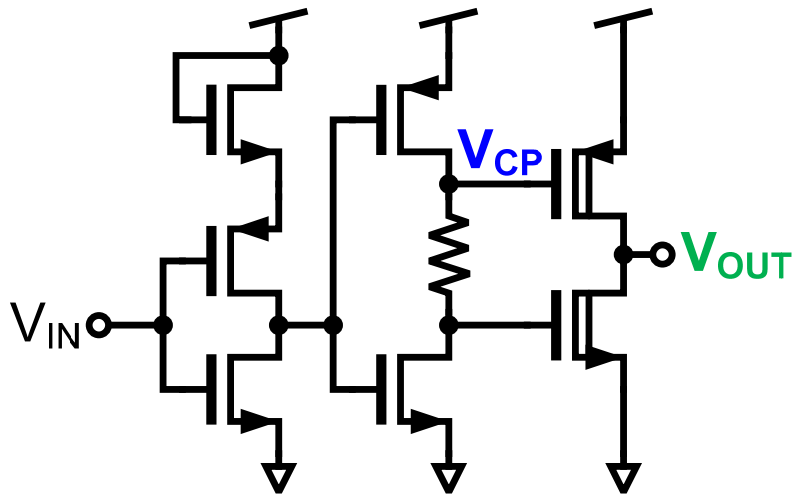
- **Second stage output V_{CP}**
 - Amplification direction ➔ **next stage sub-ADC**

Sampling Capacitor Reset Switch



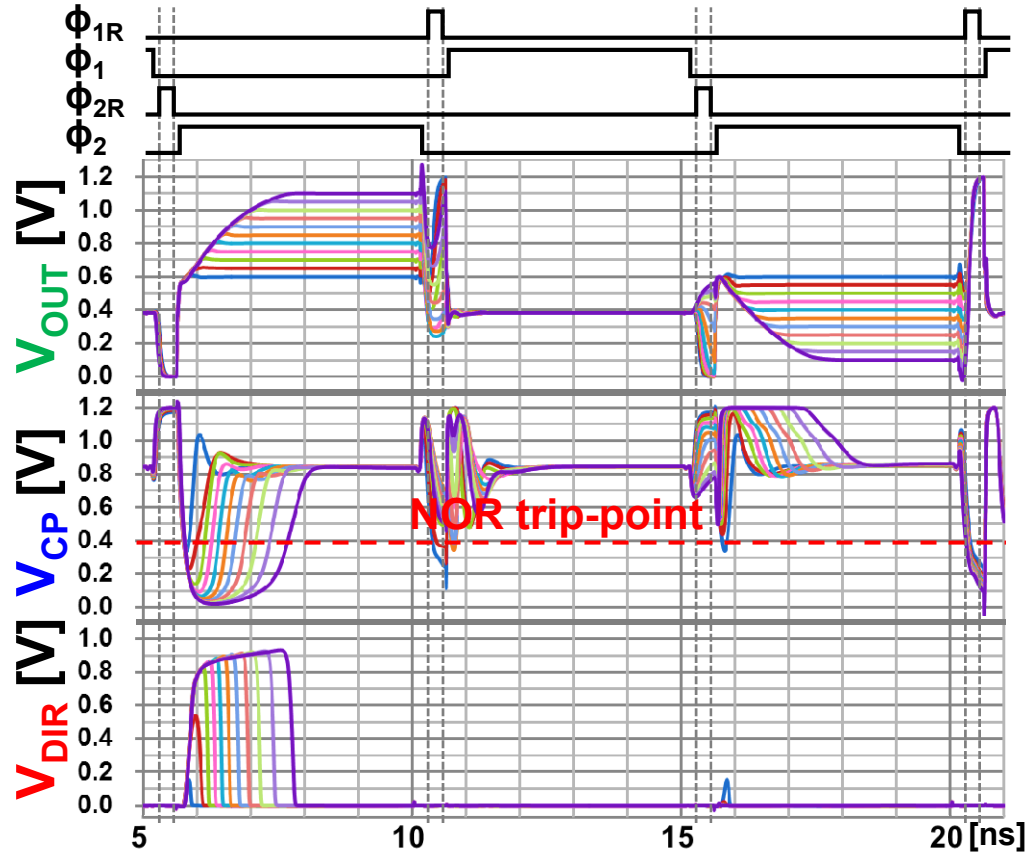
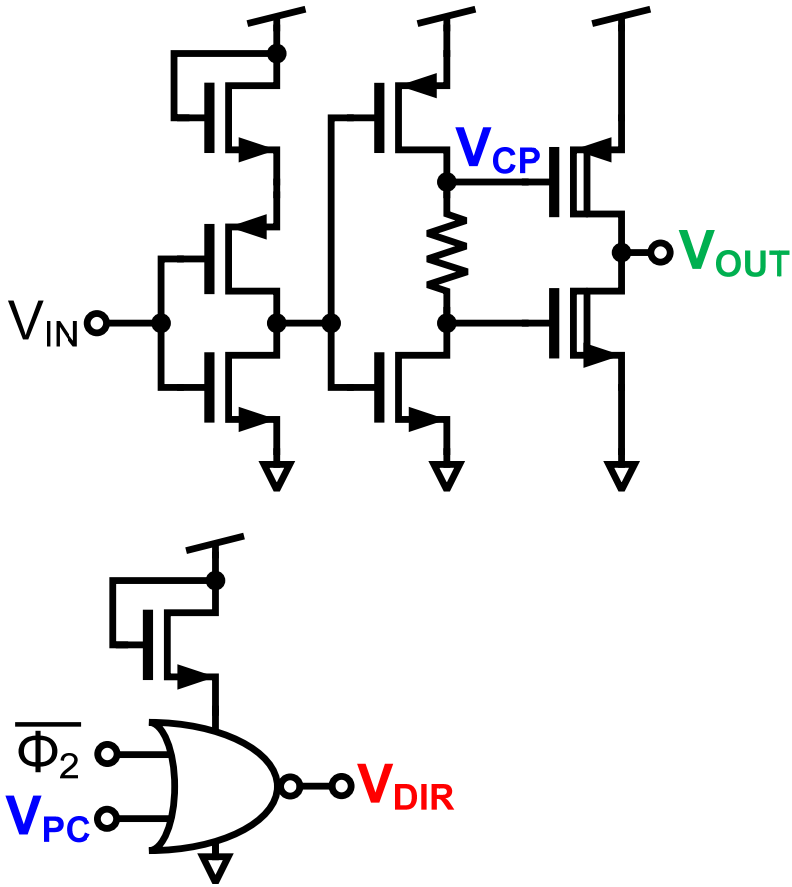
- Insure each amplification starts from V_{CM}
 - Reduce maximum slew requirement by 1/2

Comparator-less Sub-ADC



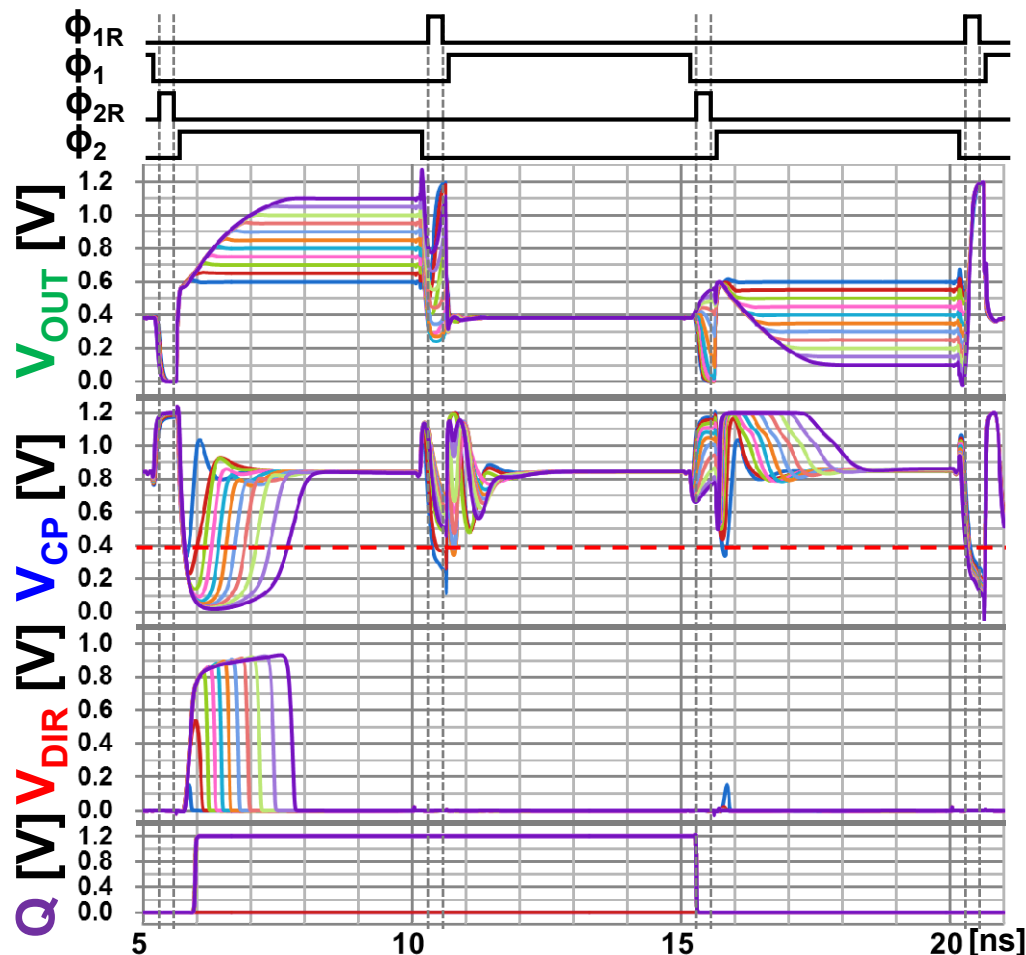
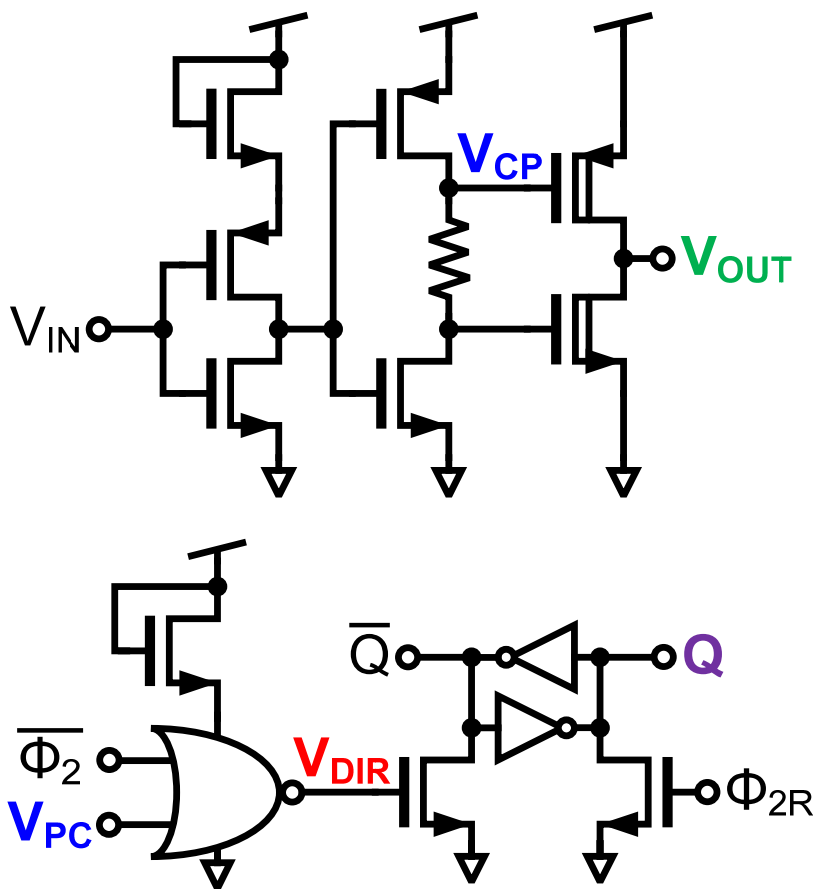
➤ Amplification direction sampling

Comparator-less Sub-ADC



- **Amplification direction sampling**
 - Low trip-point NOR

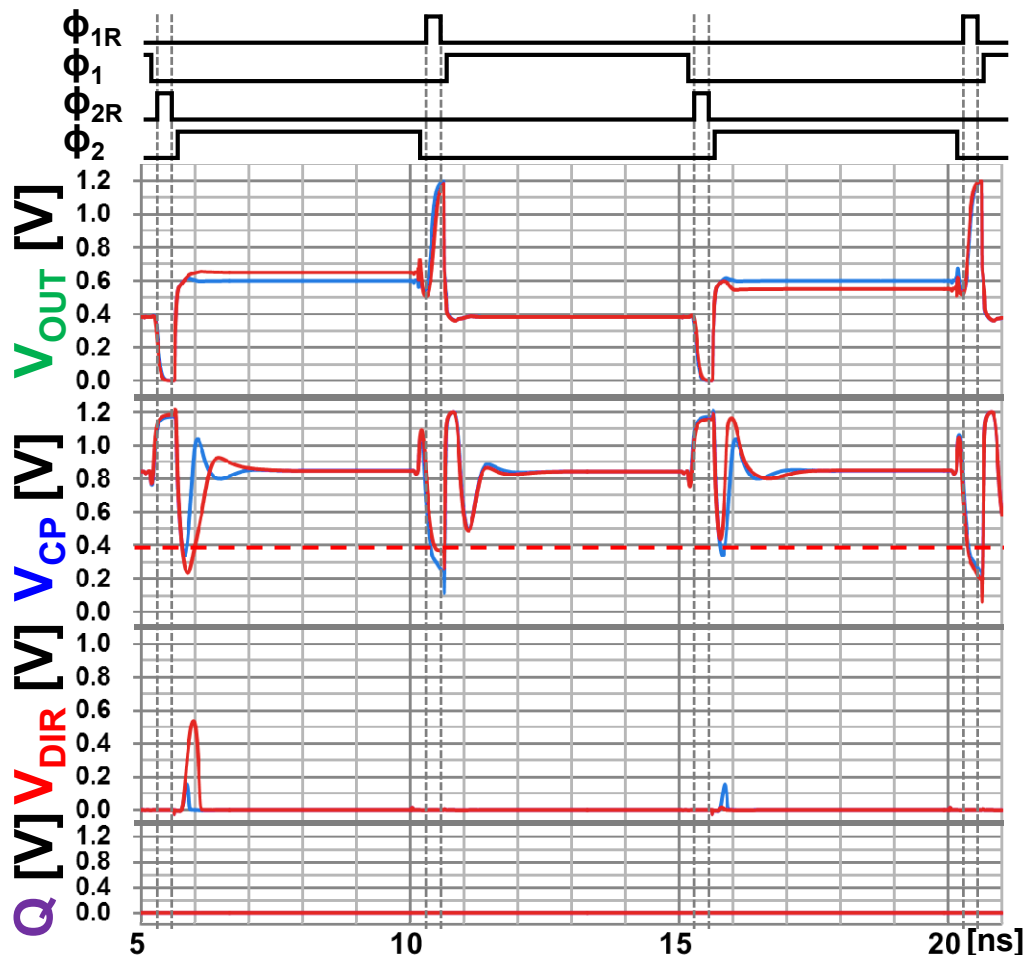
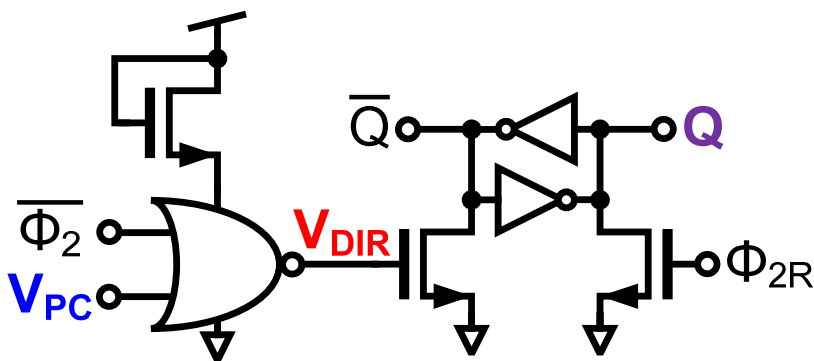
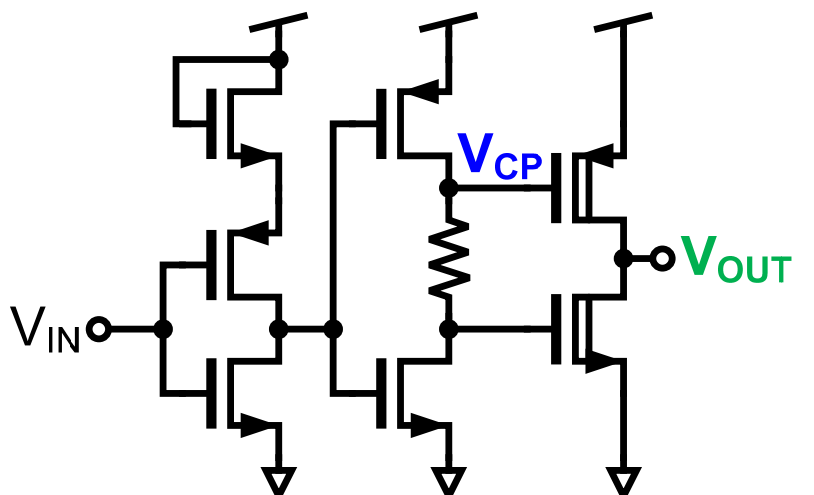
Comparator-less Sub-ADC



➤ Amplification direction sampling

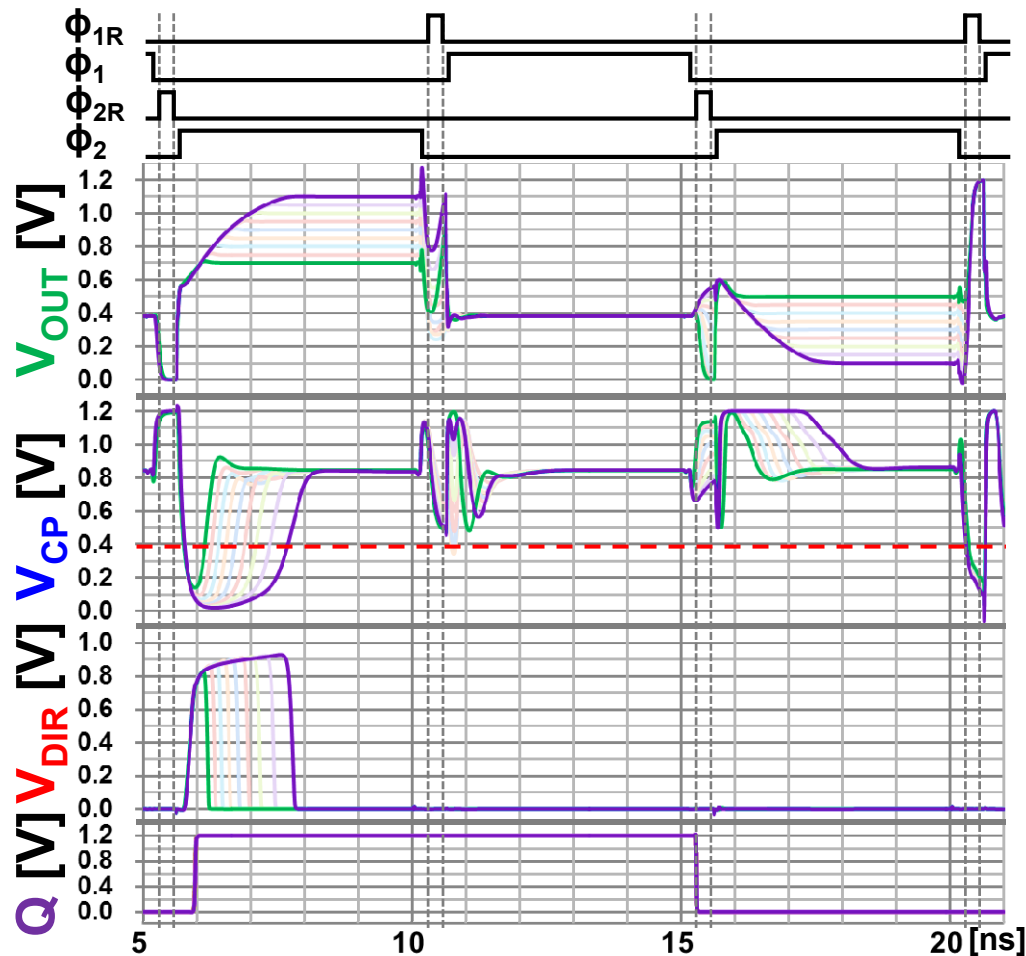
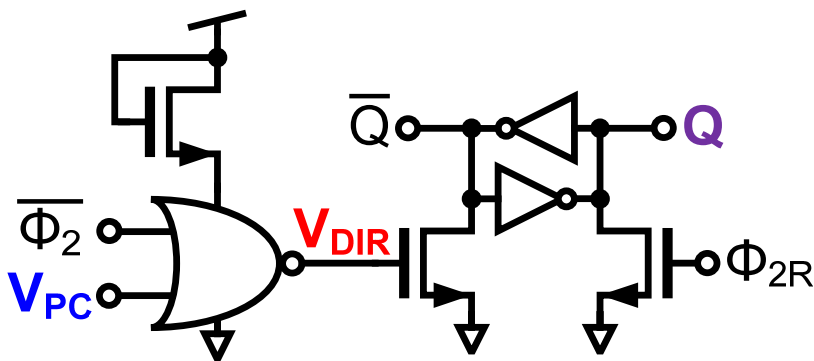
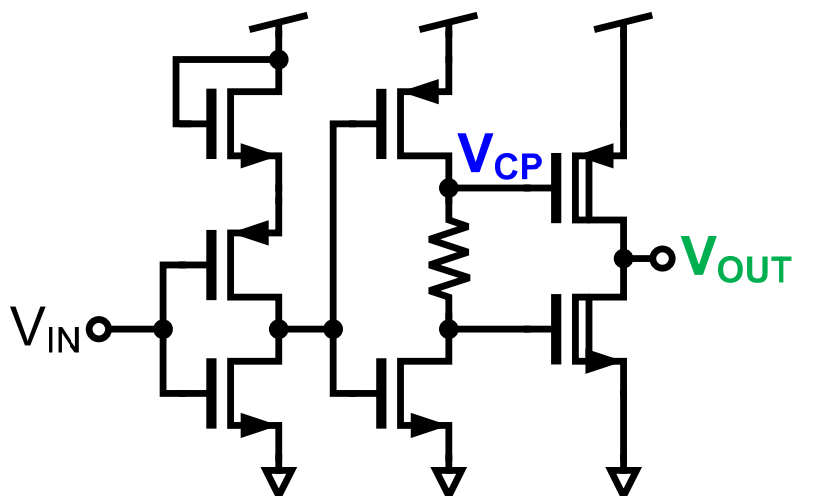
- Low trip-point NOR + SR latch

Comparator-less Sub-ADC



➤ $V_{OUT} < 0.65V \rightarrow Q = 0$

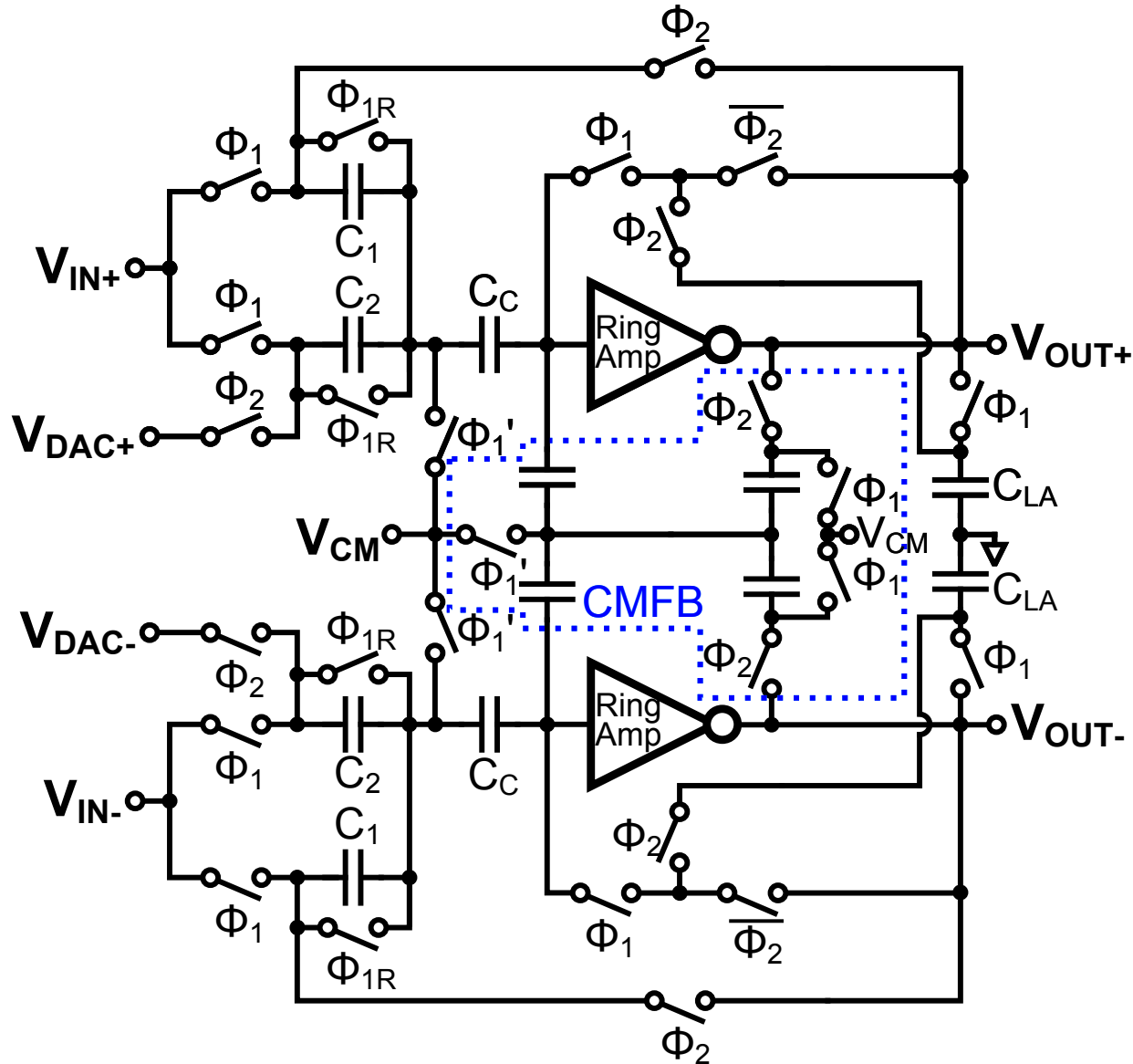
Comparator-less Sub-ADC



➤ $V_{OUT} > 0.7V \rightarrow Q = 1$

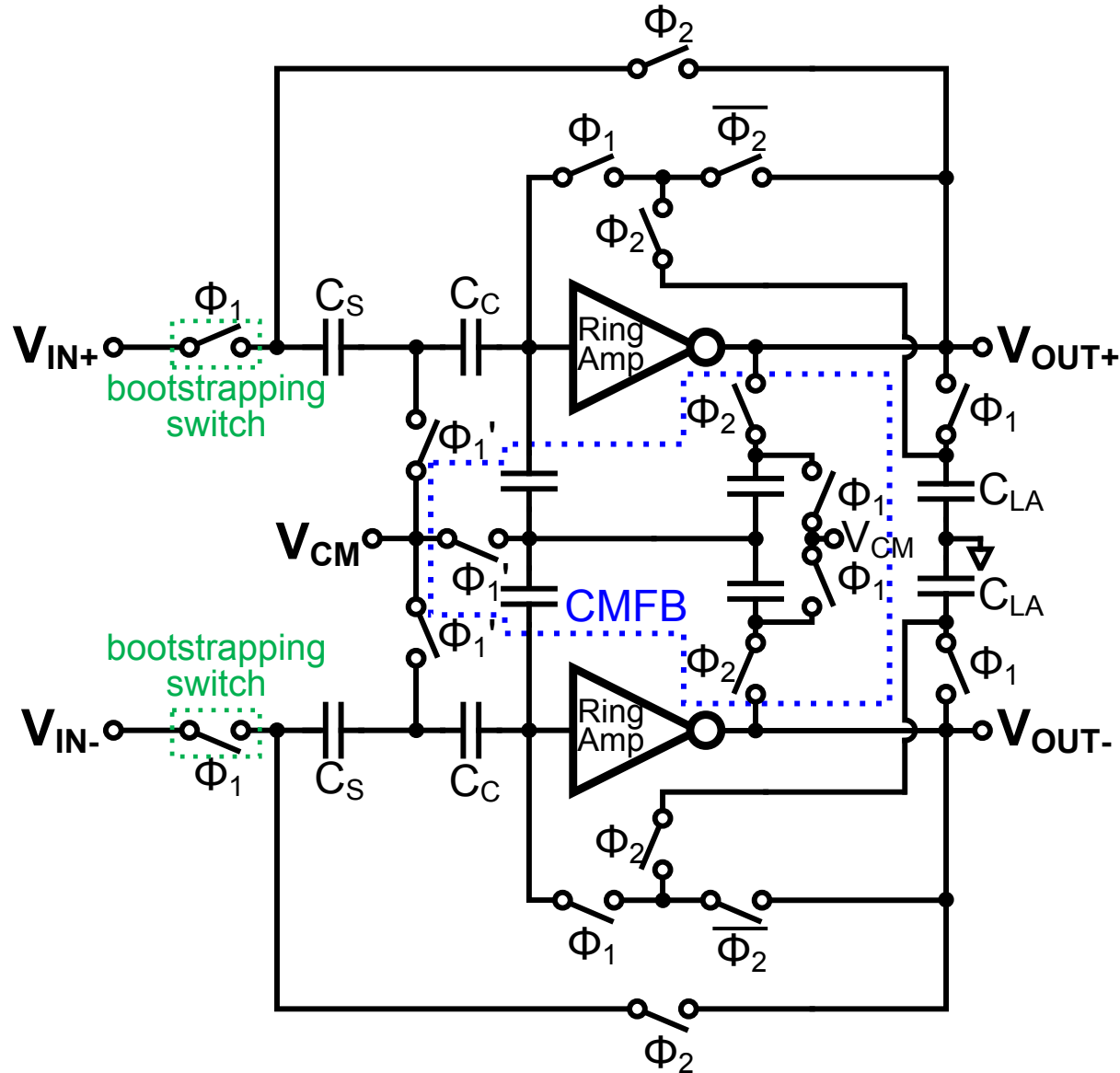
■ Effective comparator threshold $\approx 0.675V$

Pseudo-differential MDAC



CMFB: [Hershberg, ISSCC 2012]

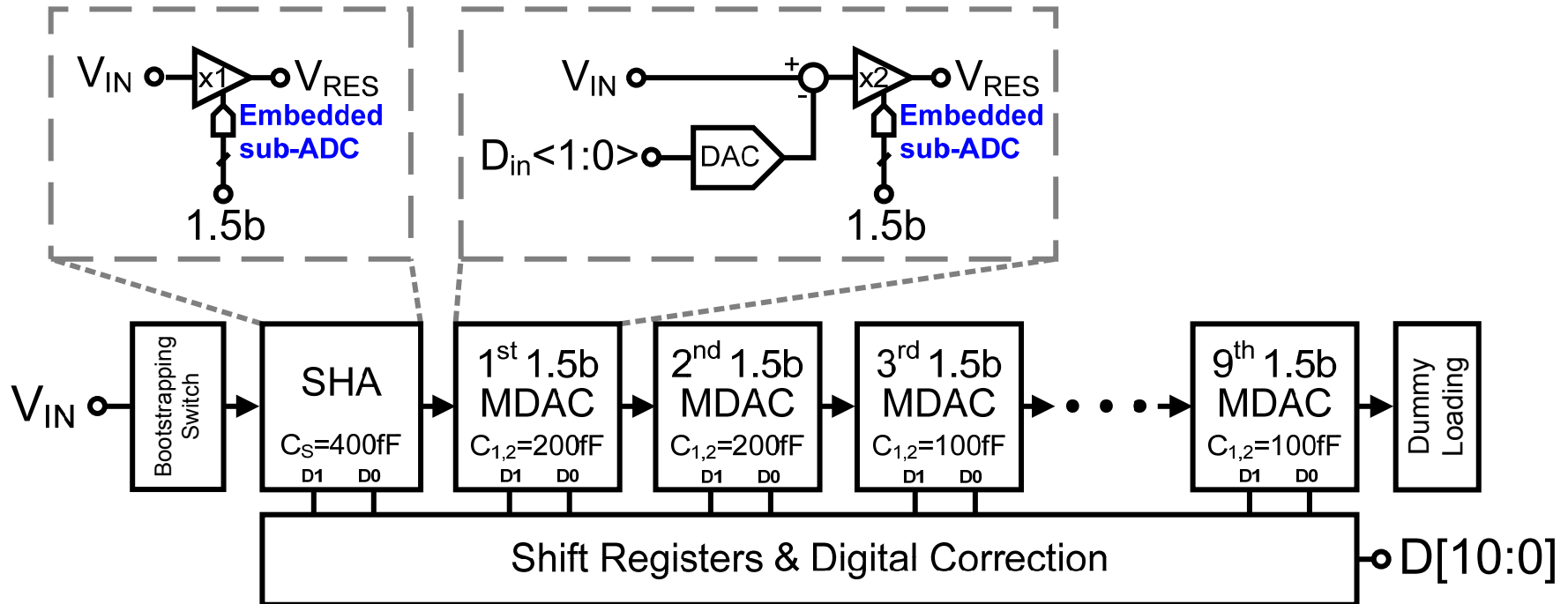
Flip-around SHA (also First sub-ADC)



Bootstrapping switch: [Abo, JSSC 1999]

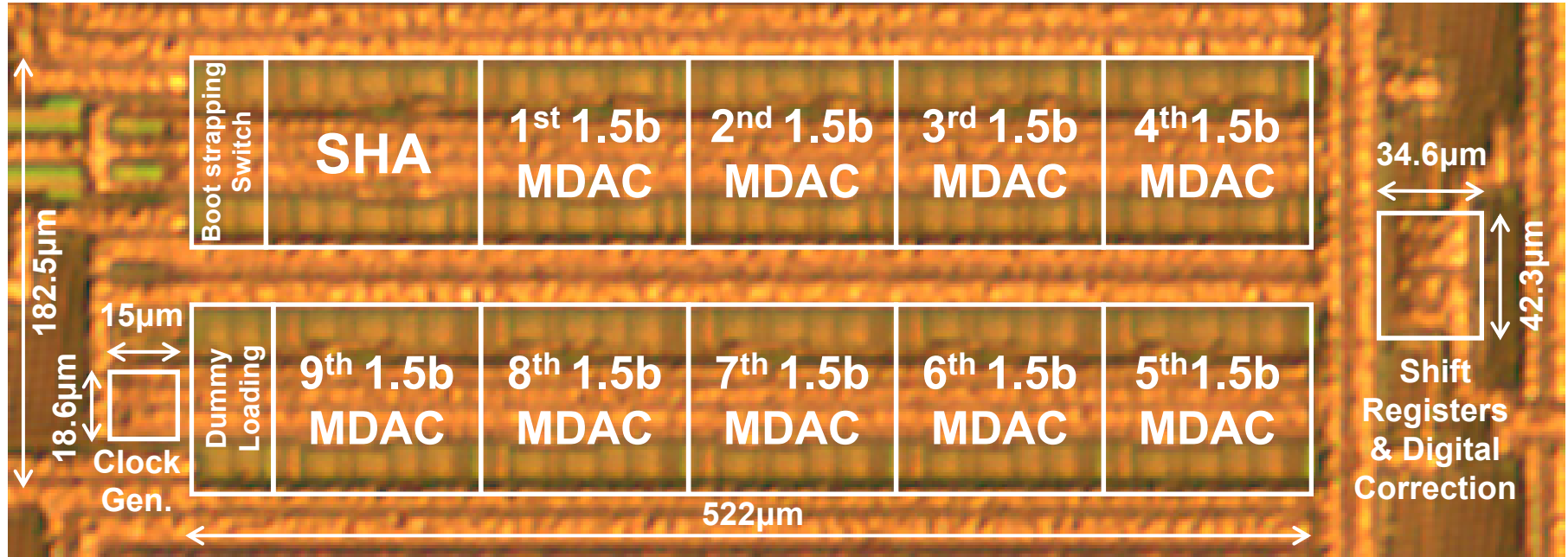
ADC Implementation

10.5b 100MSPS Pipeline ADC



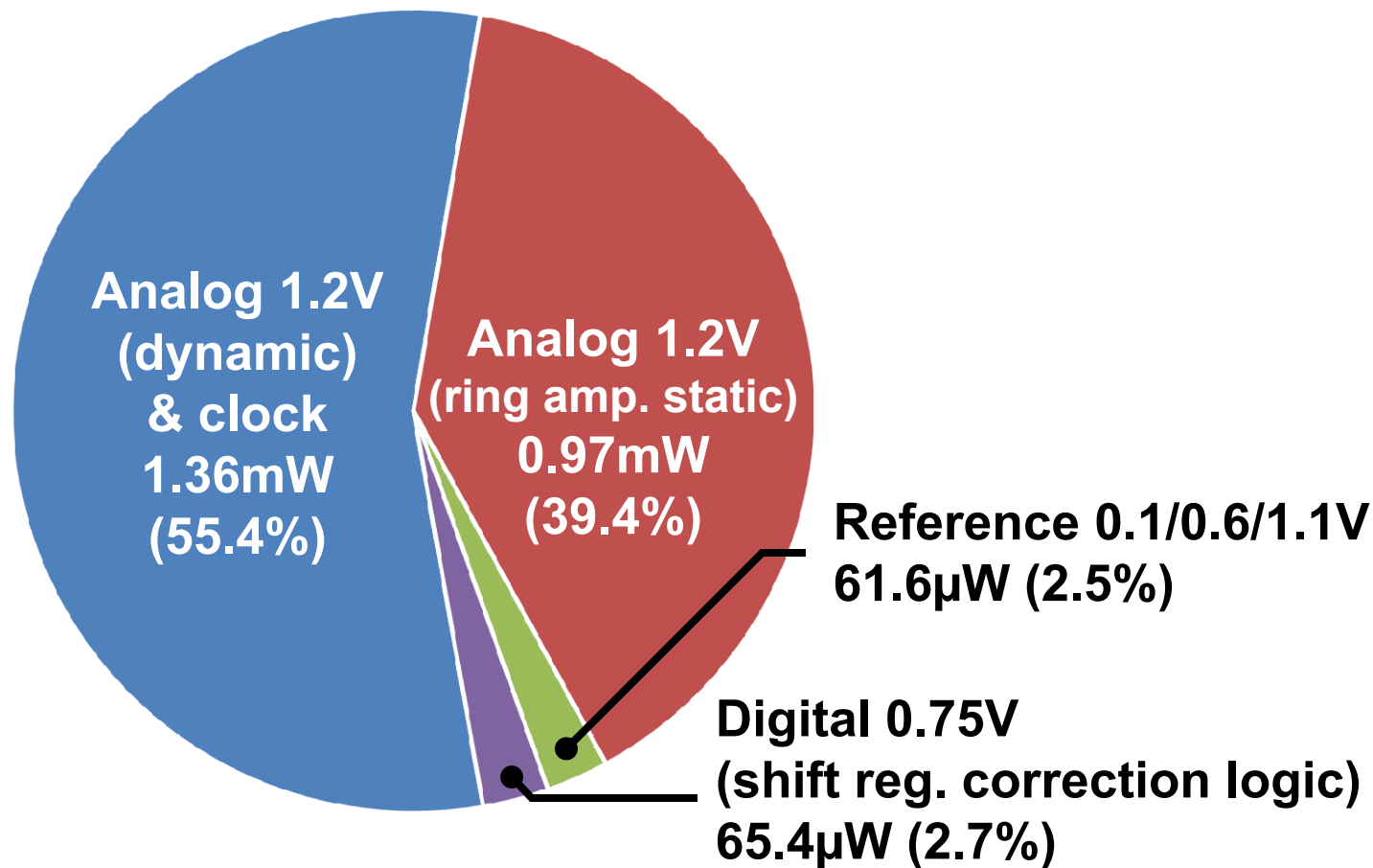
➤ Ring amp SHA + nine 1.5b MDAC + dummy loading

ADC Die Photo



- **65nm CMOS process**
 - Active area: 0.097mm²

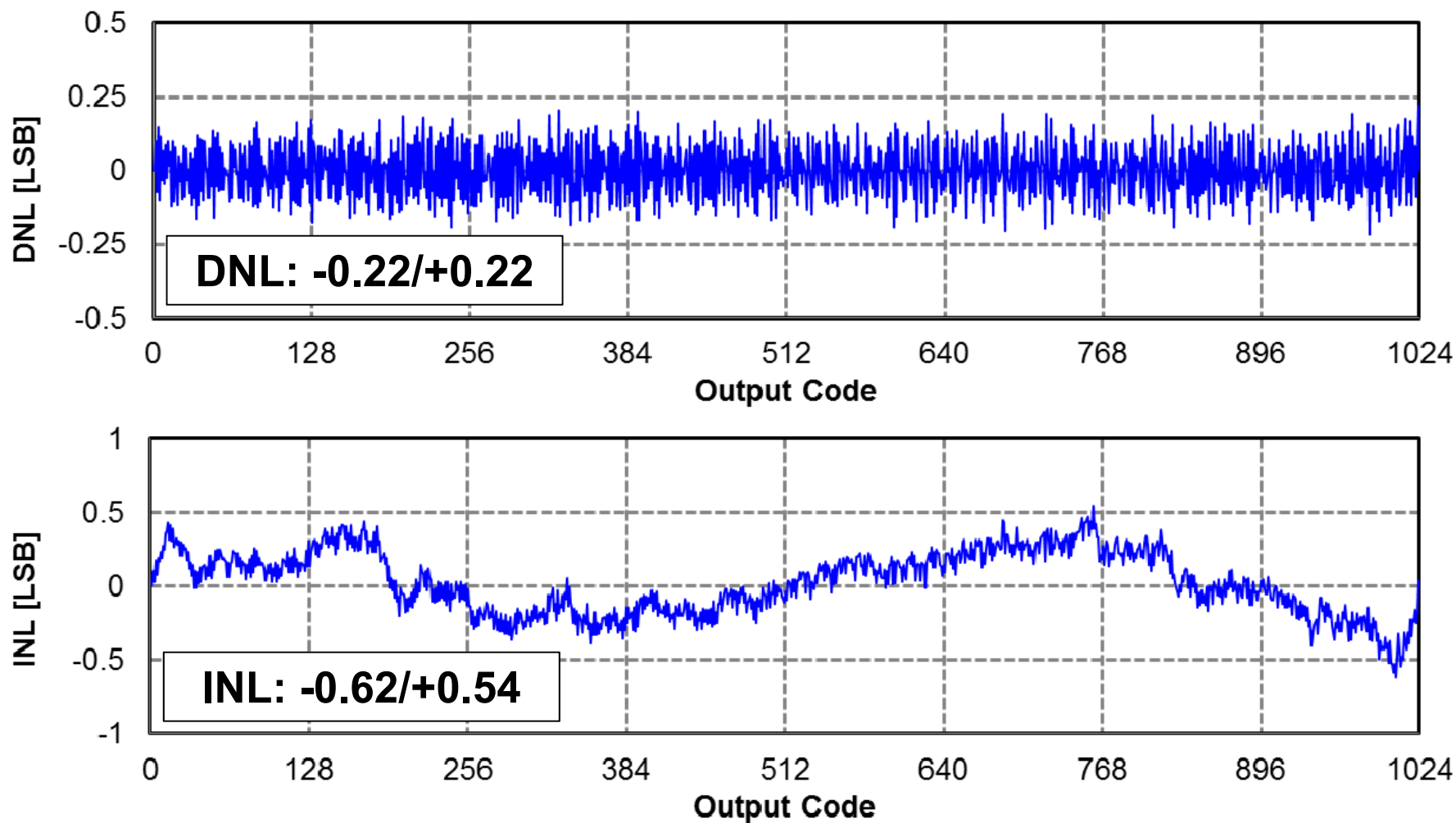
Measured Power Consumption



➤ **Total 2.46mW at 100MS/s operation**

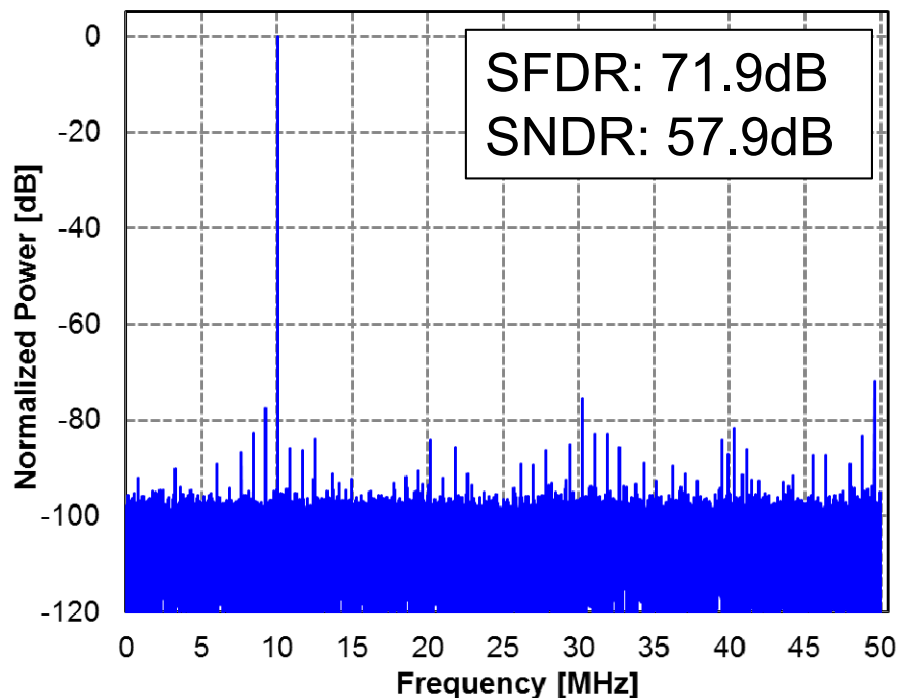
■ Ring amplifier quiescent current: 60μA, 32μA

Measured DNL & INL at 100MS/s

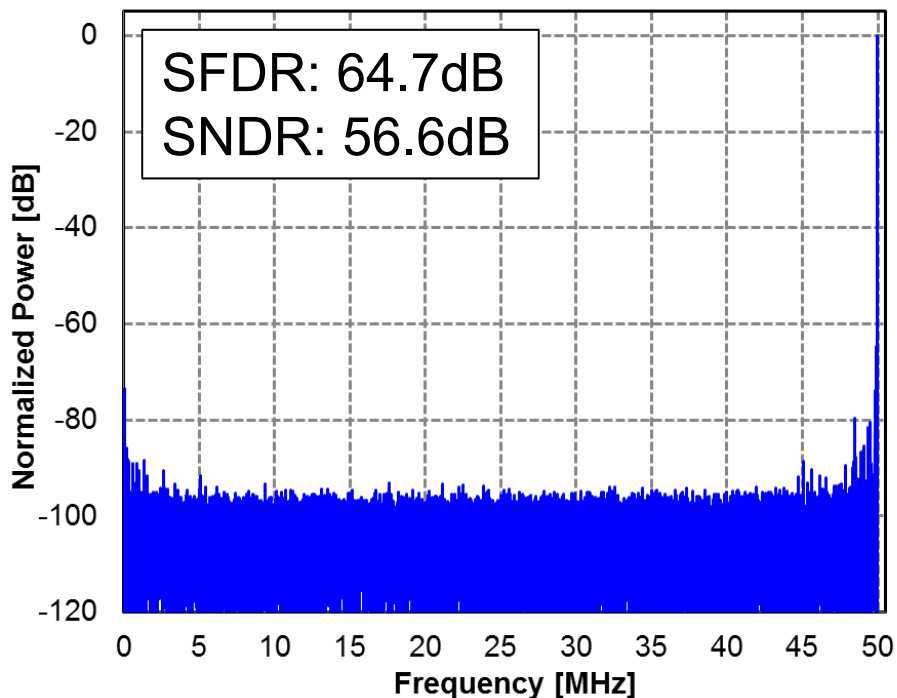


Measured Spectrum at 100MS/s

$F_{in} = 10.08\text{MHz}$

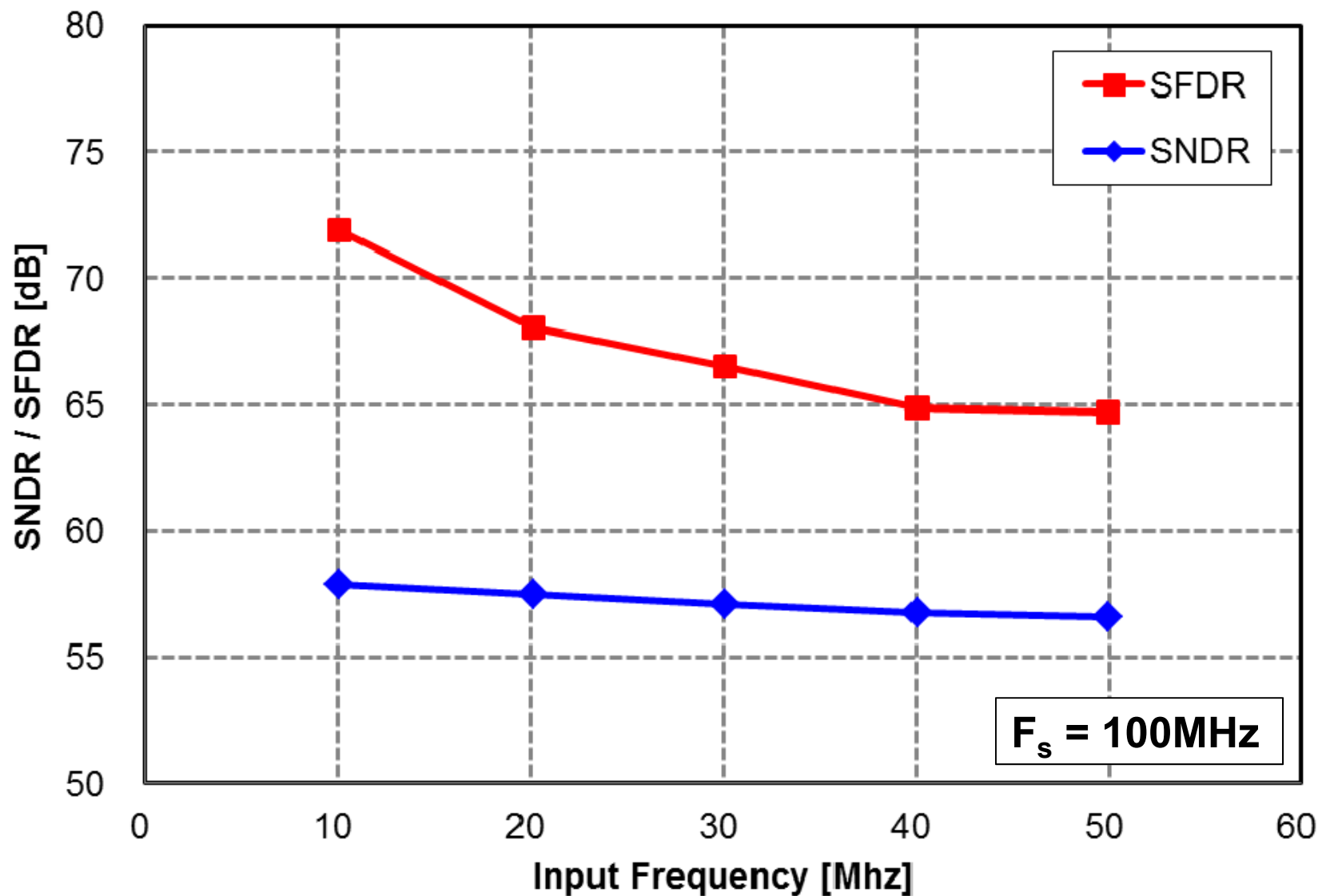


$F_{in} = 49.97\text{MHz}$

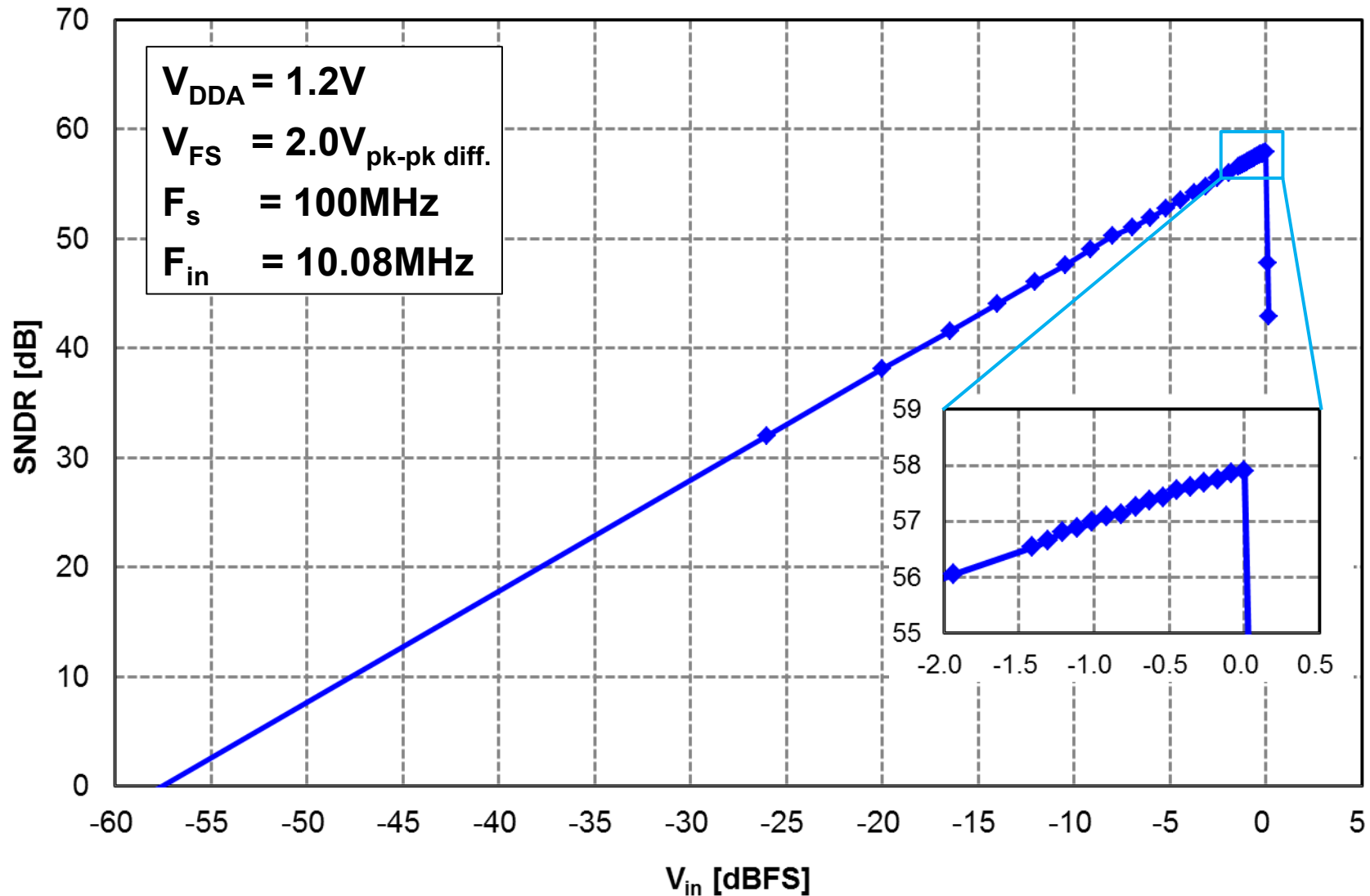


* 65,536 point FFT

Dynamic Performance

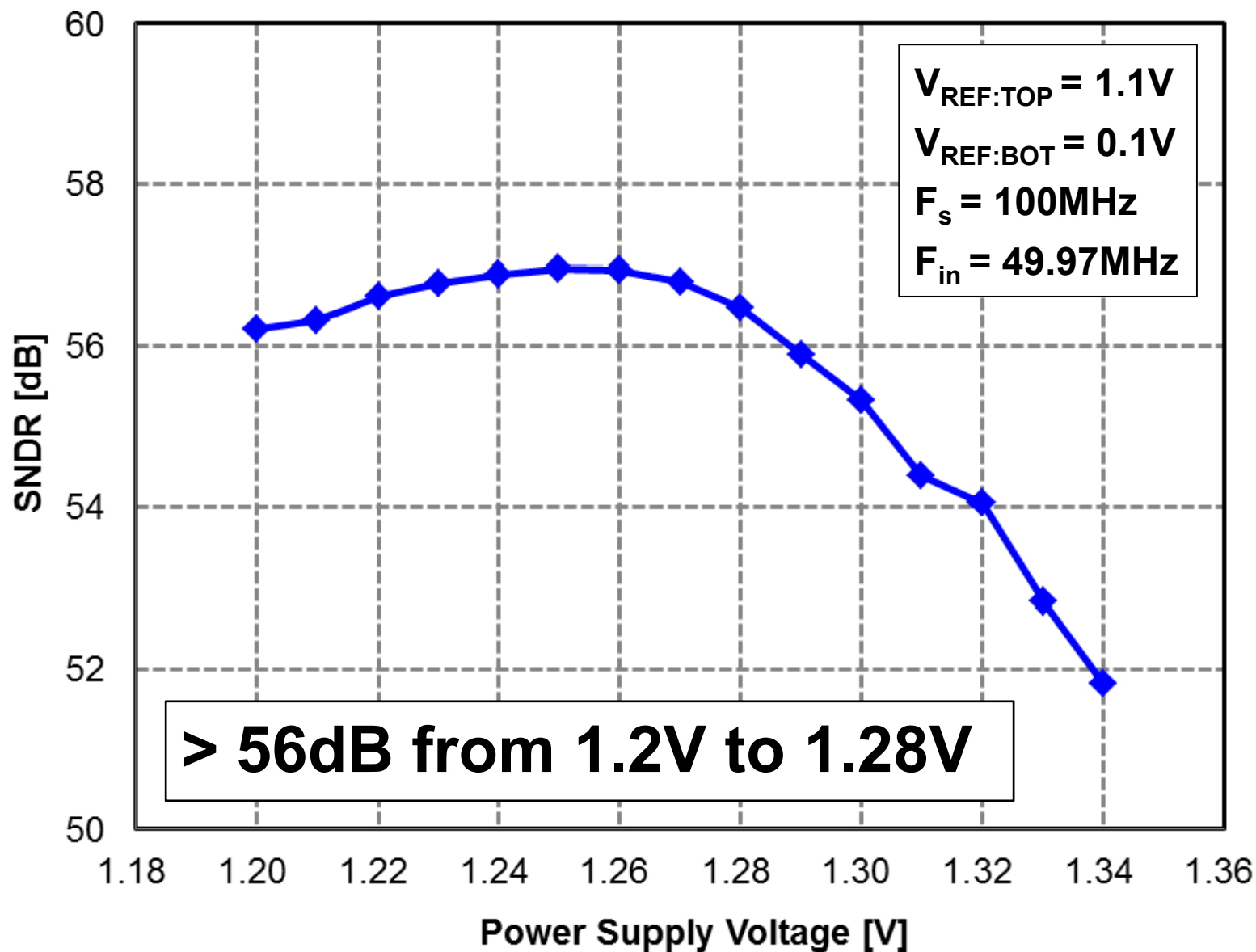


SNDR vs. Input Amplitude



➤ Linear up to full scale

SNDR vs. Analog Power Supply



Measurement Summary

Resolution	10.5 bits	
Supply	1.2V (Analog, Clock), 0.75V (Digital)	
Sampling Rate	100MS/s	
Technology	65nm 1P9M CMOS	
Active Area	0.097mm ²	
Input Range	2.0V _{pk-pk} differential	
DNL (10 bits)	-0.22/+0.22LSB	
INL (10 bits)	-0.54/+0.62LSB	
Power Consumption	2.46mW Total 2.33mW (Analog + Clock), 61.6μW (Ref.), 65.4μW (Digital)	
	F_{in}=10.08MHz	F_{in}=49.97MHz
SNDR	57.9dB	56.6dB
SNR	58.2dB	57.5dB
SFDR	71.9dB	64.7dB
ENOB	9.33bits	9.11bits
FoM [P/(f_s · 2^{ENOB})]	38.4fJ/conv-step	44.5fJ/conv-step

Performance Comparison

		This Work	Hershberg, VLSI 2012	Hershberg, ISSCC 2012	Hershberg, VLSI 2013
Resolution		10.5bits	10.5bits	15bits	15bits
Sampling Rate		100MSPS	30MSPS	20MSPS	20MSPS
ADC Architecture		1.5b/stage	1.5b/stage	3b/stage	3b/stage
Amp. Structure		Self-biased ring amp only	Ring amp only	Ring amp + split-CLS	Coarse + fine ring amplifier
Technology		65nm CMOS	180nm CMOS	180nm CMOS	180nm CMOS
Active Area		0.097mm ²	0.50mm ²	1.98mm ²	1.98mm ²
Peak result	ENOB	9.33bits	9.9bits	12.5bits	12.3bits
Nyquist freq.	ENOB	9.11bits	~9.18bits (from JSSC 2012 graph)	~11.83bits (from JSSC 2012 graph)	-
Total Power		2.46mW	2.6mW	5.1mW	2.96mW
FoM (peak result)		38.4fJ/conv-step	90fJ/conv-step	45fJ/conv-step	29fJ/conv-step
FoM (Nyquist input freq.)		44.5fJ/conv-step	149.4fJ/conv-step	70fJ/conv-step	-

Performance Comparison

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Performance Comparison

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Conclusion

- **Ring amplifier without external biasing**
 - Practical and more power efficient
- **Improved Auto-zero switching**
 - Eliminates parasitic capacitor gain error
- **Comparator-less sub-ADC**
 - Free sub-ADC using ring amplifier
- ➔ **State-of-the-art FOM for pipeline ADC**
 - 44.5fJ/conv-step, $f_{in}=49.97\text{MHz}$ @ 100MS/s

A 21mW 15b 48MS/s Zero-Crossing Pipeline ADC in 0.13 μ m CMOS with 74dB SNDR

Dong-Young Chang¹, Carlos Muñoz², Denis Daly², Soon-Kyun Shin², Kevin Guay², Thomas Thurston², Hae-Seung Lee³, Kush Gulati², Matthew Straayer²

¹Maxim Integrated, San Jose, CA,

²Maxim Integrated, North Chelmsford, MA,

³Massachusetts Institute of Technology, Cambridge, MA

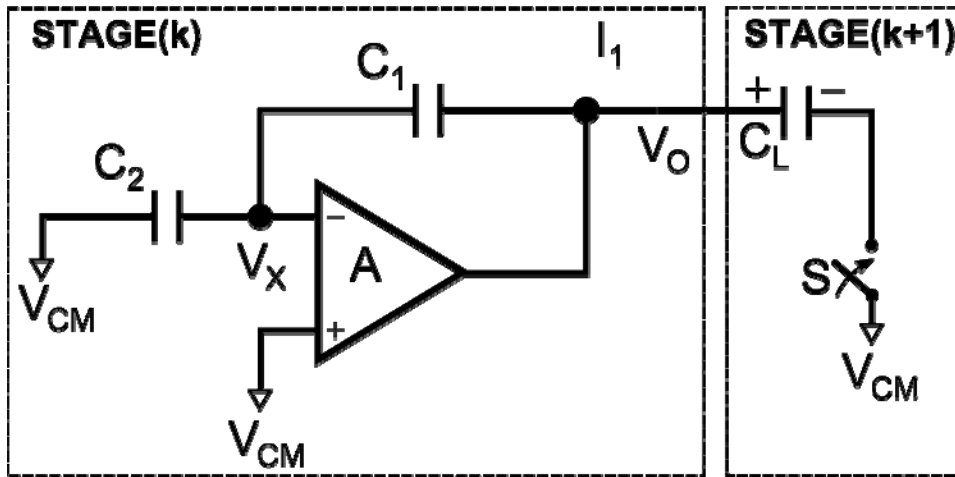
Outline

- **Overview: Zero-Crossing based Circuits (ZCBC)**
- **ZCBC ADC Challenges**
- **ADC Architecture**
- **Linearity Enhancement**
 - **Coarse Phase Threshold Control**
 - **Reference Current Compensation**
- **Measurement Results**
- **Conclusions**

Outline

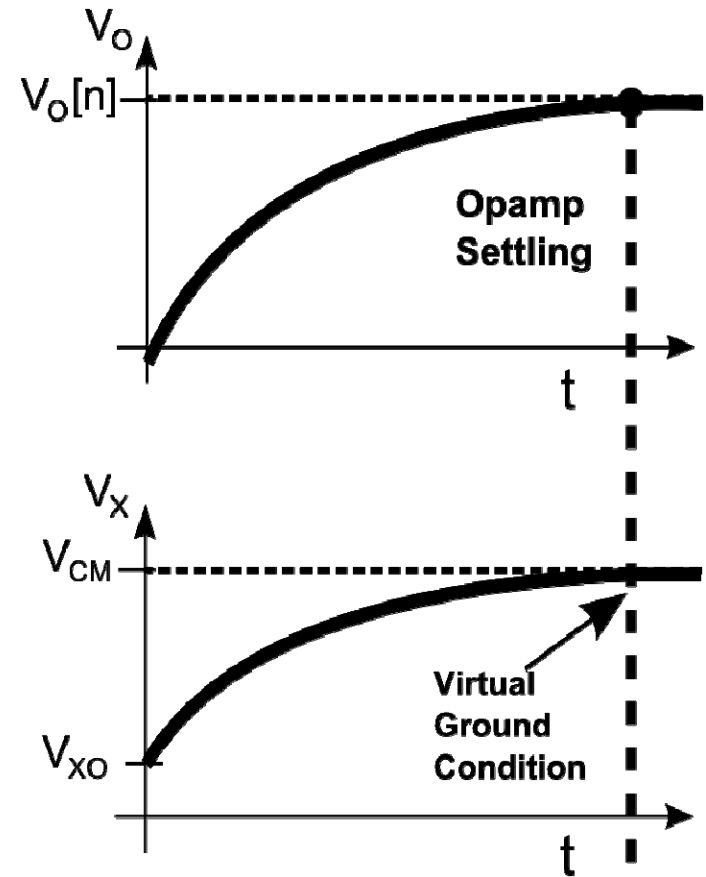
- **Overview: Zero-Crossing based Circuits (ZCBC)**
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Conventional ADC

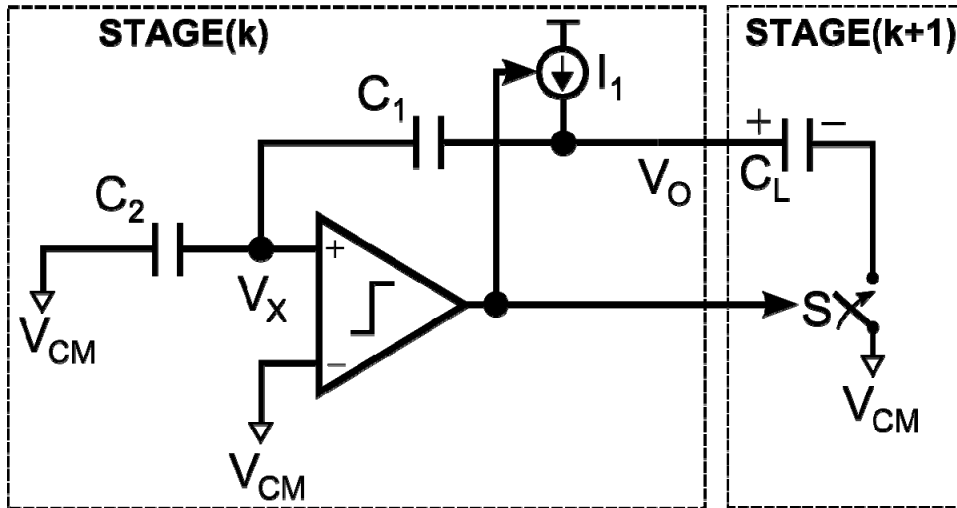


$$V_O[n] = (1 + C_2/C_1) \cdot V_{IN}[n-0.5]$$

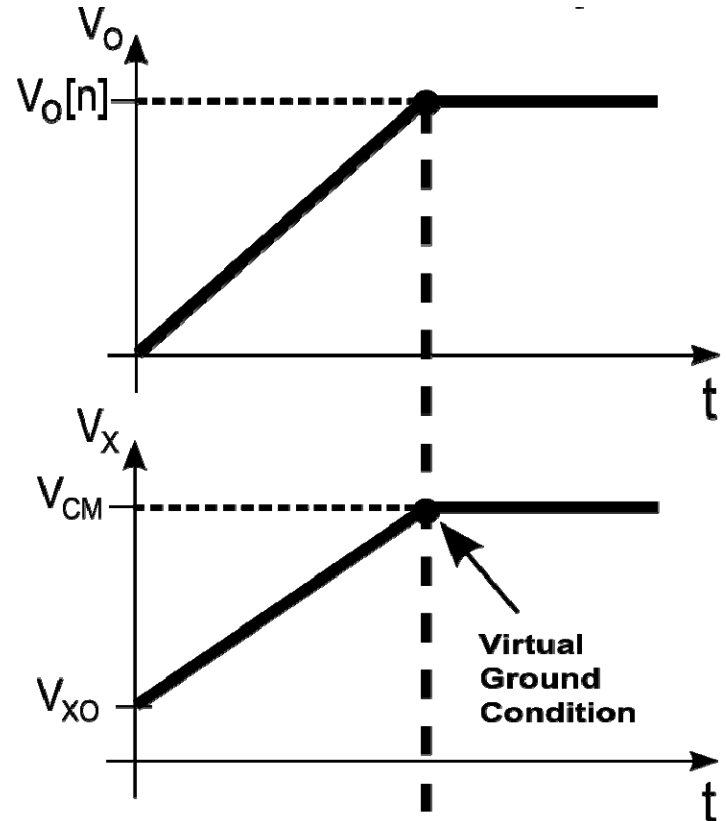
- Requires high-gain and fast opamp



ZCBC ADC



$$V_o[n] = (1 + C_2/C_1) \cdot V_{IN}[n-0.5]$$



- Z-C detector detects virtual ground condition
 - *Simple*
 - *Low-power*
 - *Amenable to deep-submicron*

Outline

- Overview: Zero-Crossing based Circuits (ZCBC)
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ZCBC ADC Challenges

- **Achieving high SNDR**
- **Headroom constraints in deep submicron processes**
- **High precision reference delivery**

ZCBC ADC Challenges

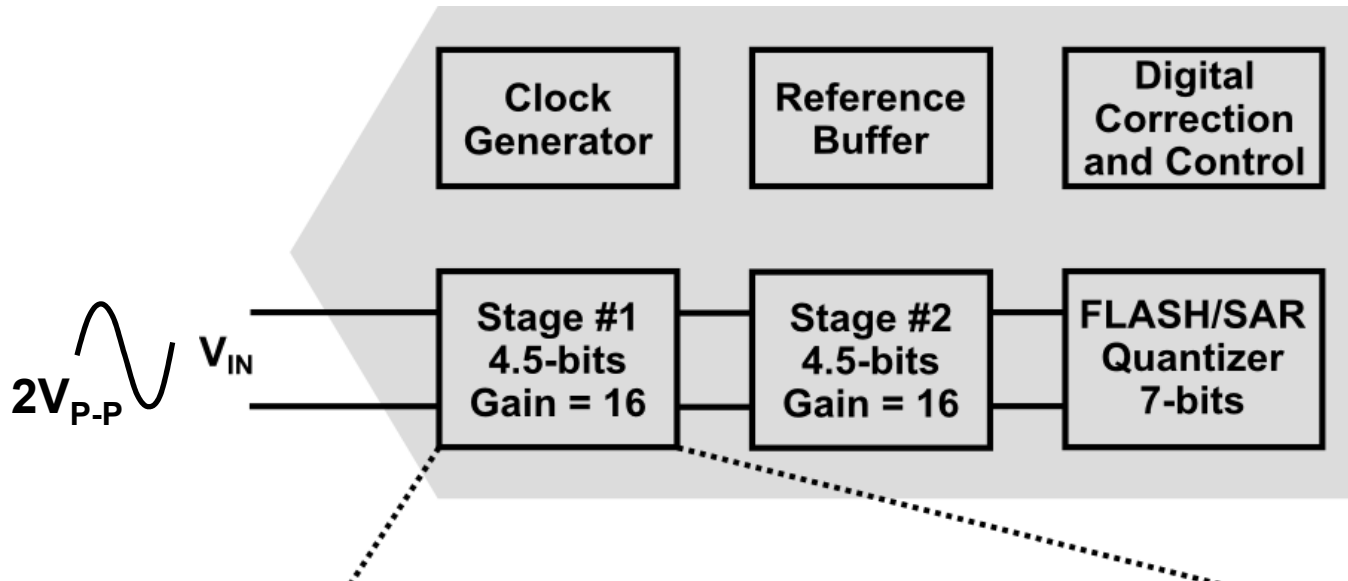
- Achieving high SNDR
 - *High resolution stage with Two-Step Sub-ADC*
 - *Dual ramp with Coarse Phase Threshold Control*
- Headroom constraints in deep submicron processes
 - *Dual ramp with Coarse Phase Threshold Control*
- High precision reference delivery
 - *Reference Current Compensation*

Outline

- Overview: Zero-Crossing based Circuits (ZCBC)
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ADC Architecture

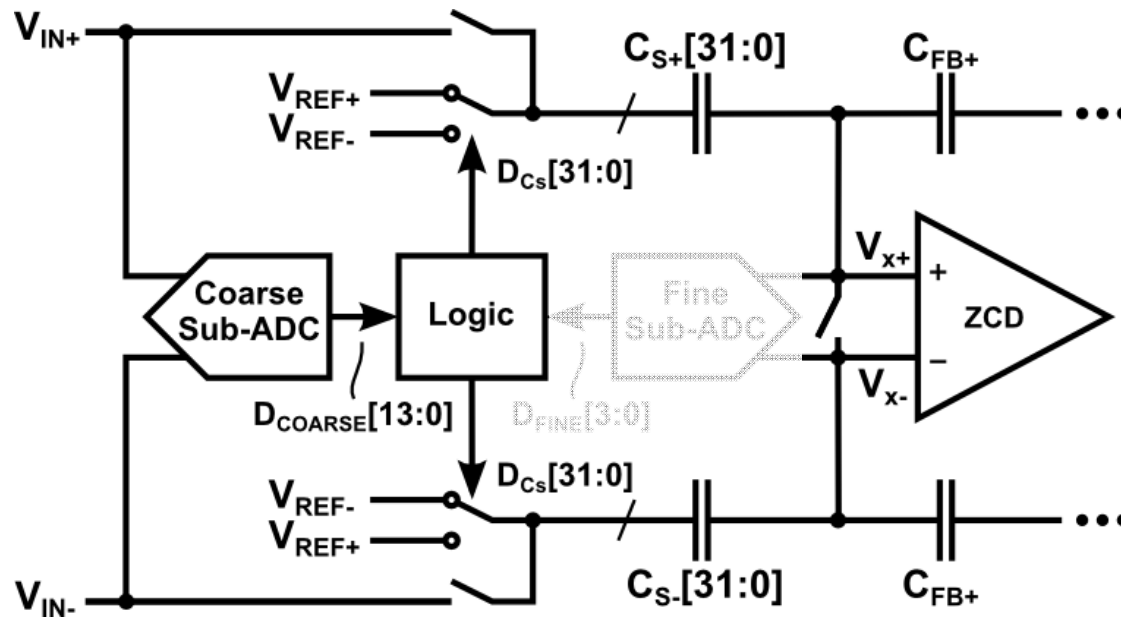
- ADC core: $V_{DD}=1.2V$, Reference Buffer: $V_{DD}=1.8V$



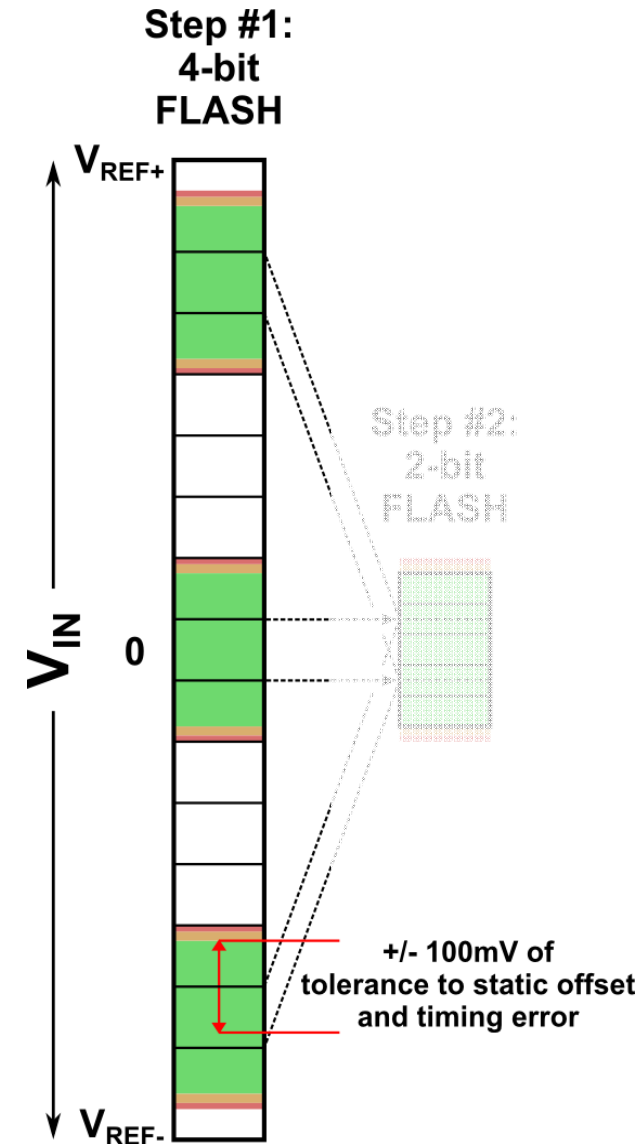
Primary Challenges:

- **Accurate comparator design**
 - Intrinsic offset limits to 3-bit FLASH
- **Timing error**
 - Limits input signal frequency

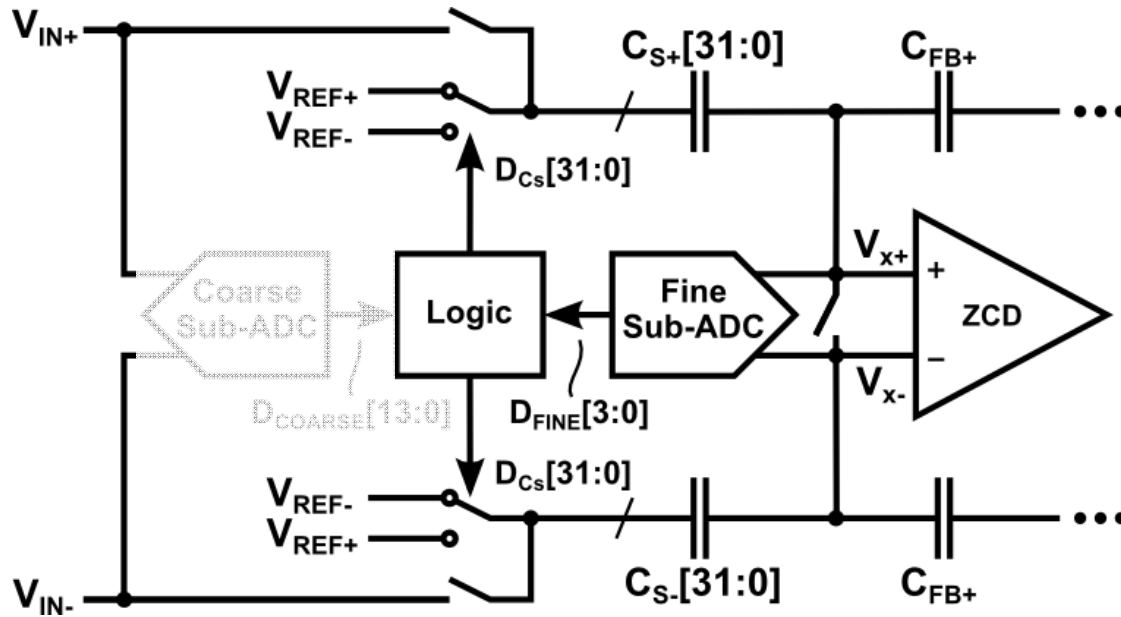
Two-Step Sub-ADC: 4-bit Coarse



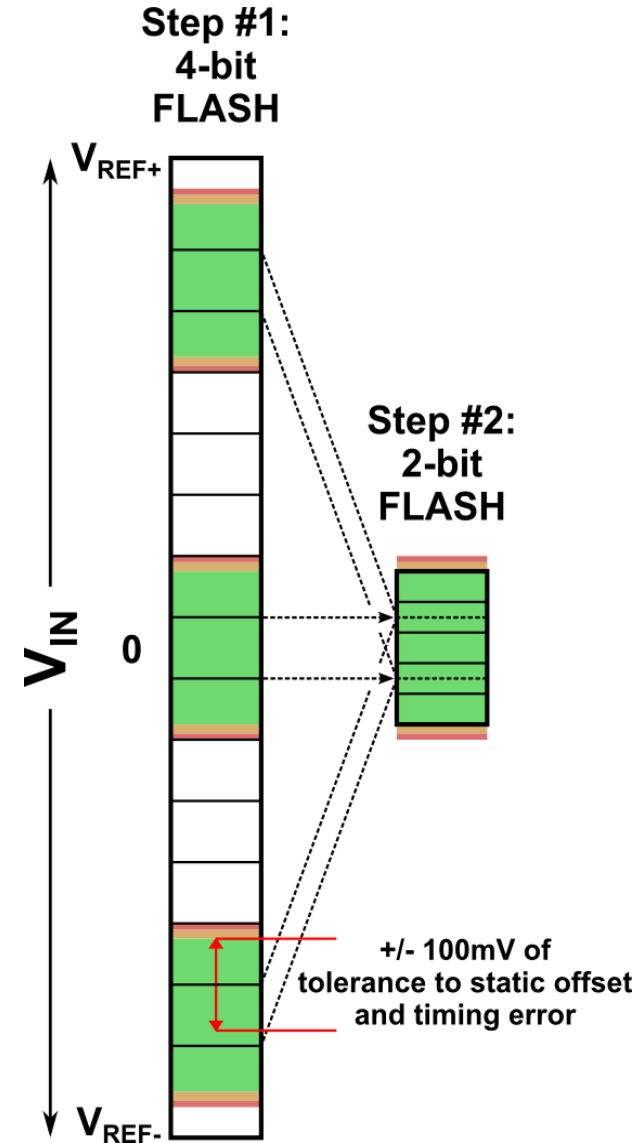
- 4-bit FLASH
- Relaxed comparator accuracy requirement



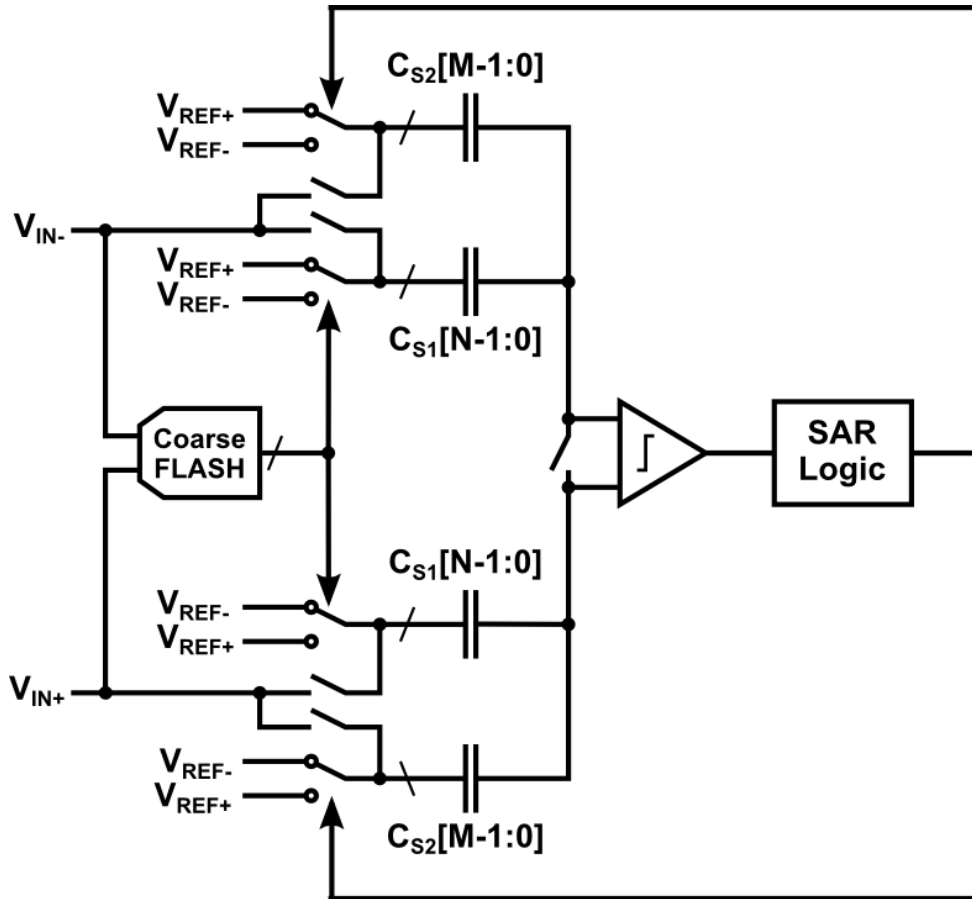
Two-Step Sub-ADC: 2-bit Fine



- **Only 4 comparators need to be accurate**
 - **Trade-off: gain error and power/area**
- **Less sensitive to timing mismatch**



7-b FLASH/SAR Quantizer

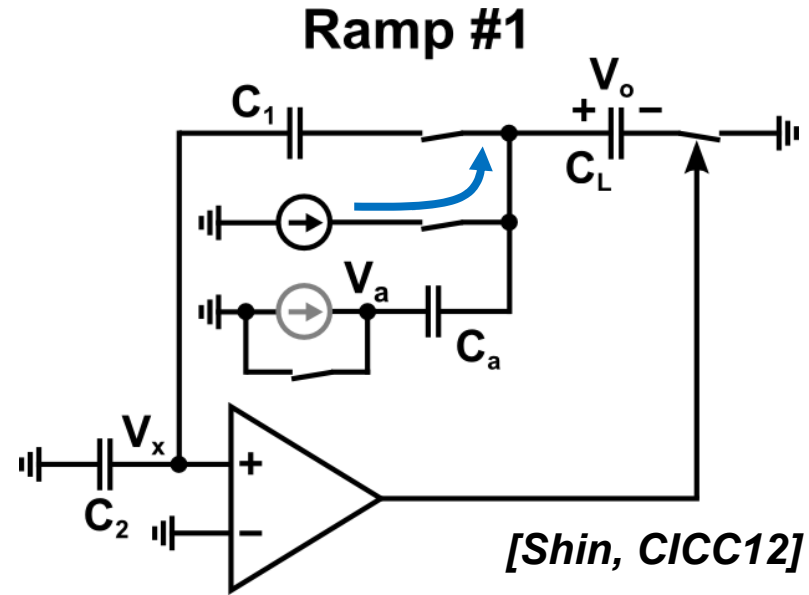
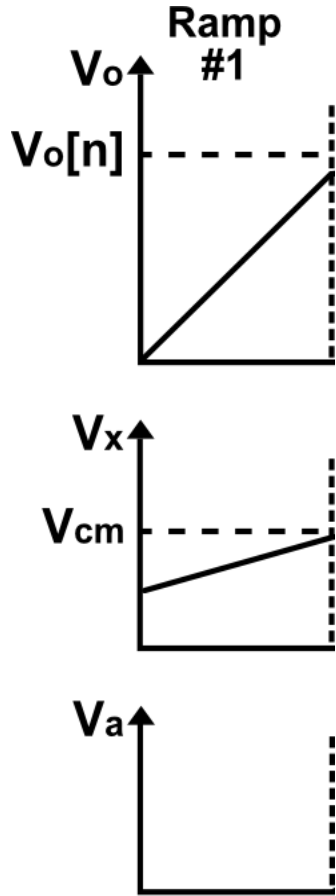


- 3.5-bit coarse FLASH decision
- 4-bit fine SAR decision with 1-bit overlap
- Dedicated reference buffer to avoid coupling
- Single comparator → Low DNL/INL w/o calibration

Outline

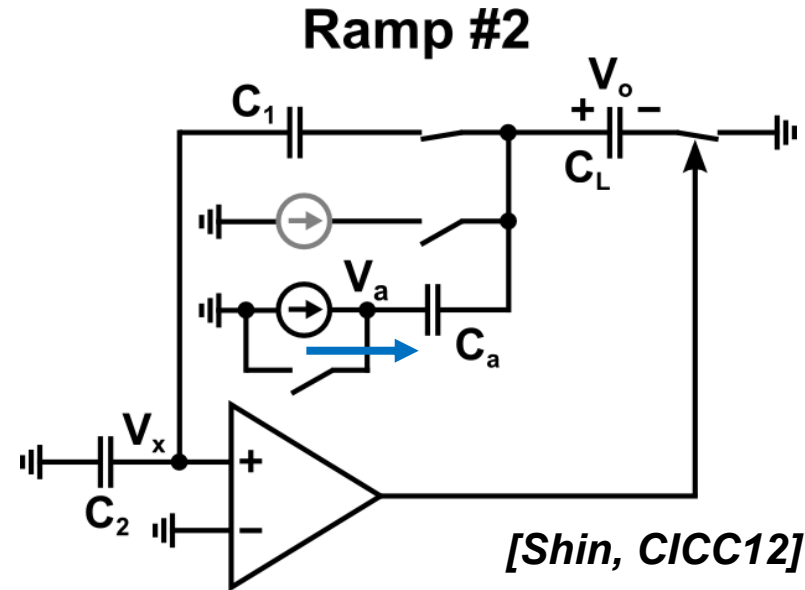
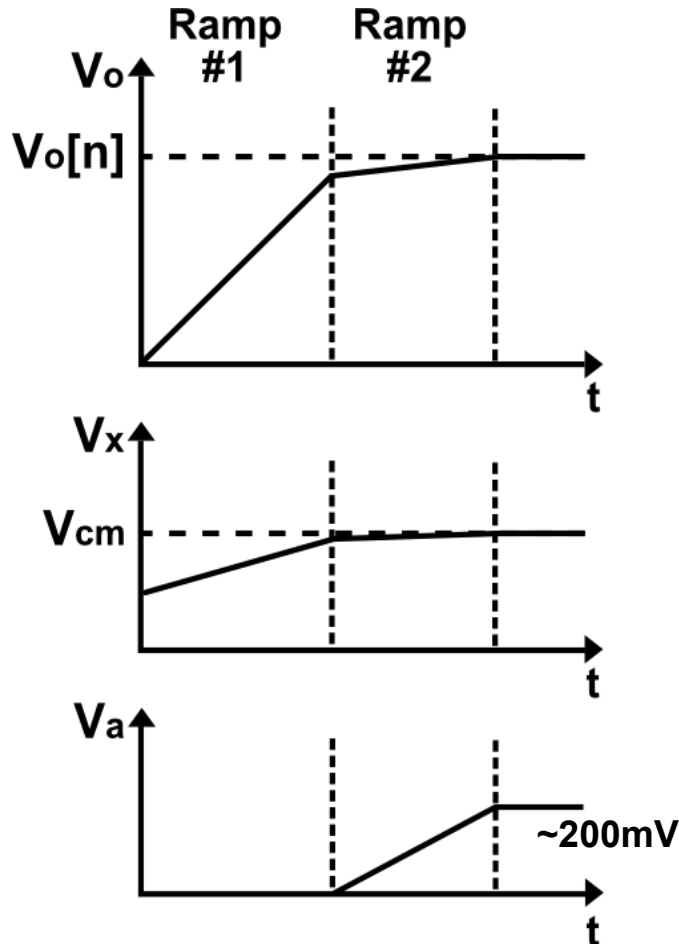
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Two-Phase Ramp: Coarse Phase



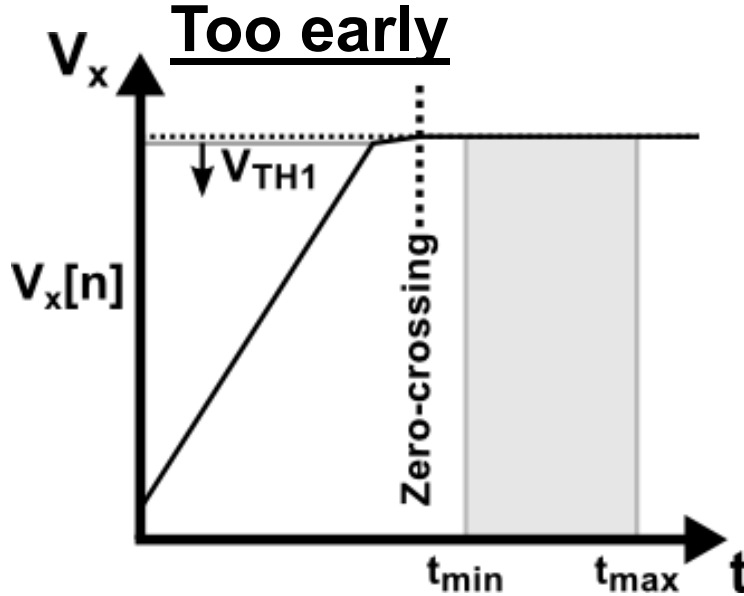
- Ramp #1: Coarse ramp current charges loading cap directly

Two-Phase Ramp: Fine Phase

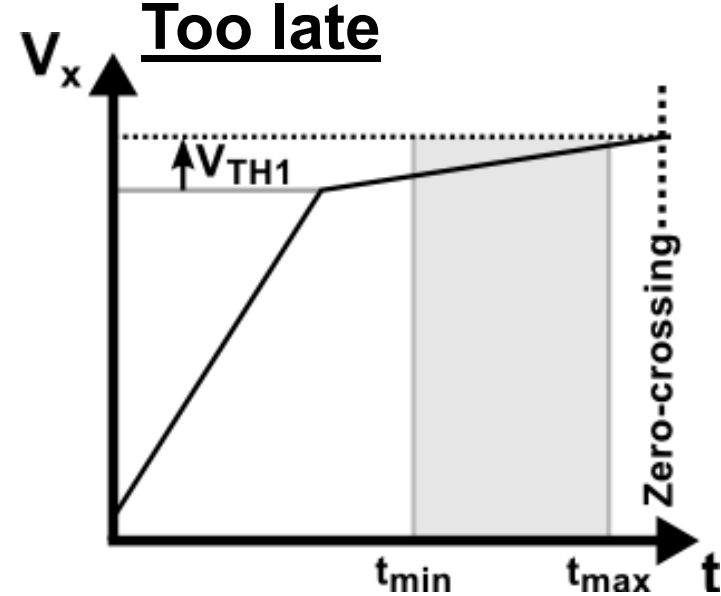


- Ramp #2: Fine ramp current through series capacitor (C_a)
 - No headroom issue
 - Ramp INL $< 0.1\text{LSB}$
- Accurate hand-over between coarse and fine is required

Coarse Phase Threshold (V_{TH1})

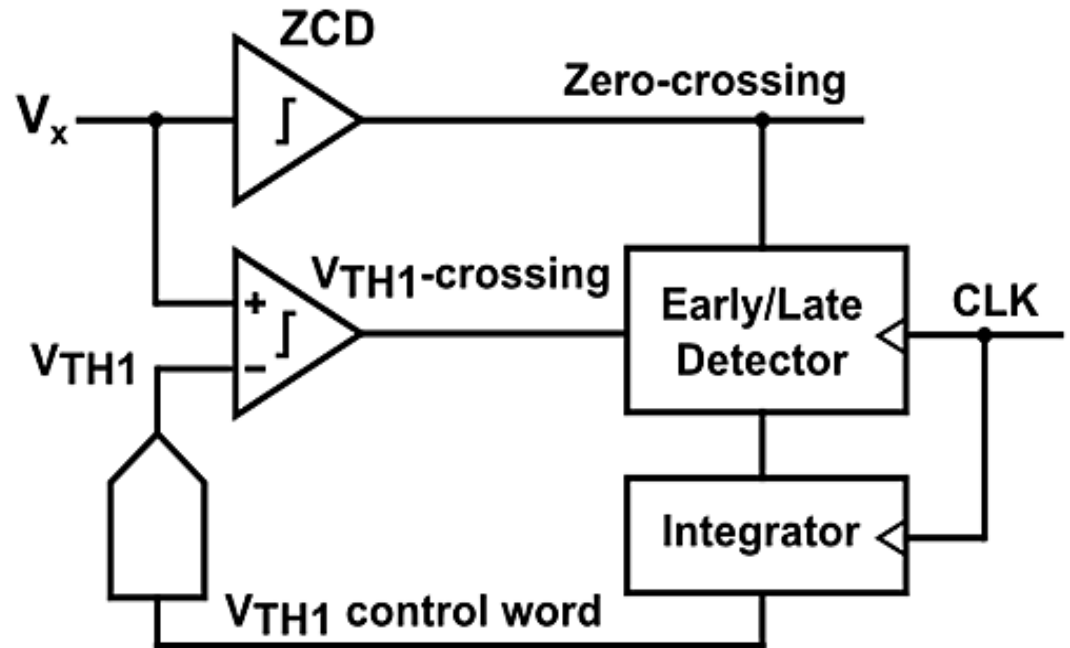
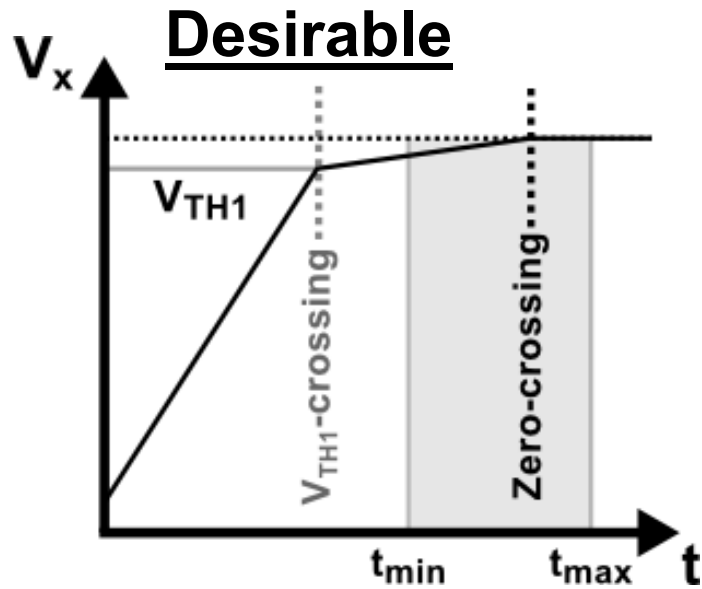


- Z-C before ZCD reaches steady state
- Phase 1 decision dominates accuracy
- Kickback during between coarse and fine transition



- Ramp linearity degrades
 - Conversion doesn't finish in time
- *Need coarse phase threshold control*

Coarse Phase Threshold Control



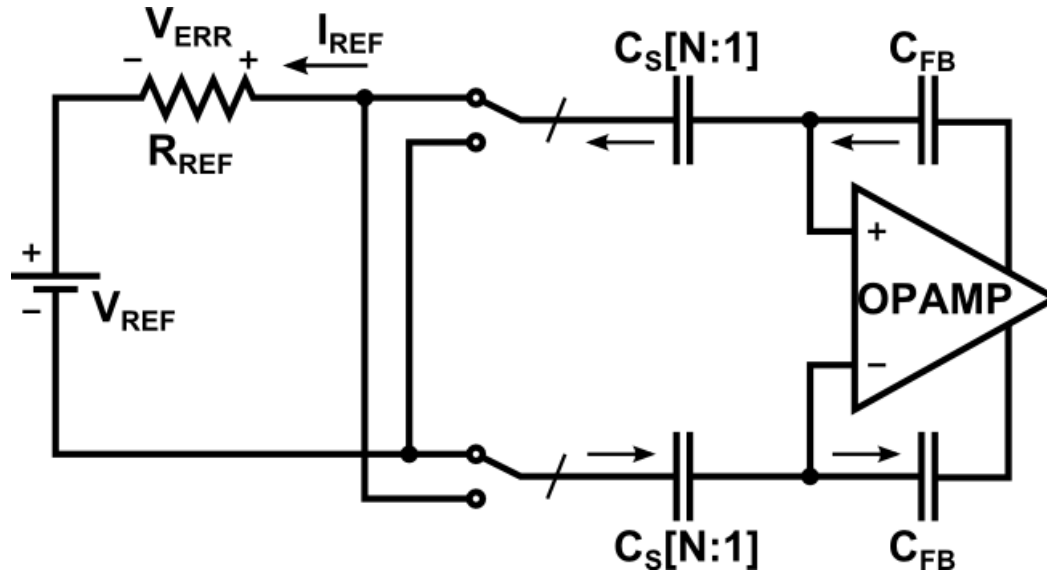
- Control loop digitally adjusts desired V_{TH1}
- Control loop runs in background
 - Sets V_{TH1} correctly over PVT

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Reference Current Challenges (1)

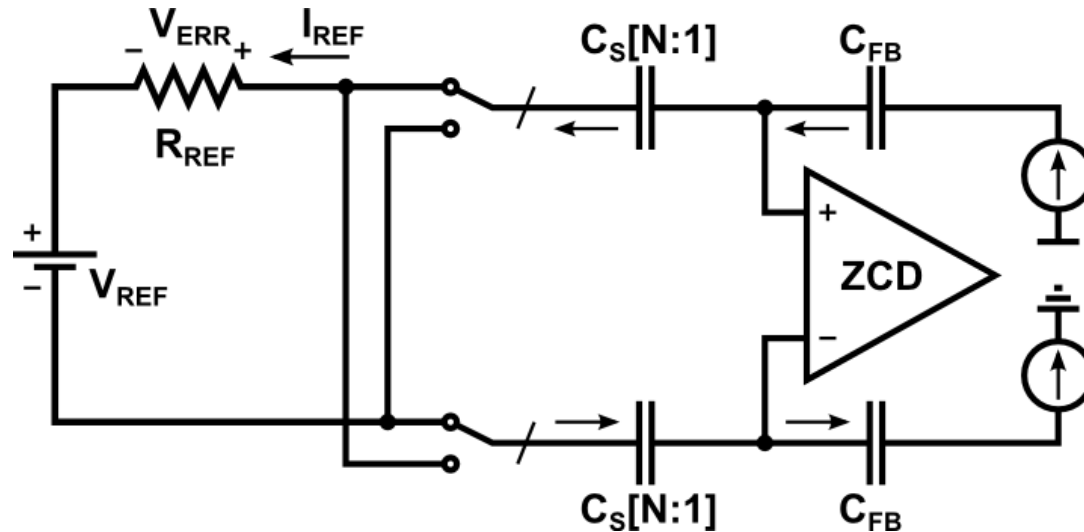
Opamp-based ADC



- I_{REF} is a function of MDAC data and time, but settles exponentially to zero during charge transfer
- No effective voltage drop across R_{REF}

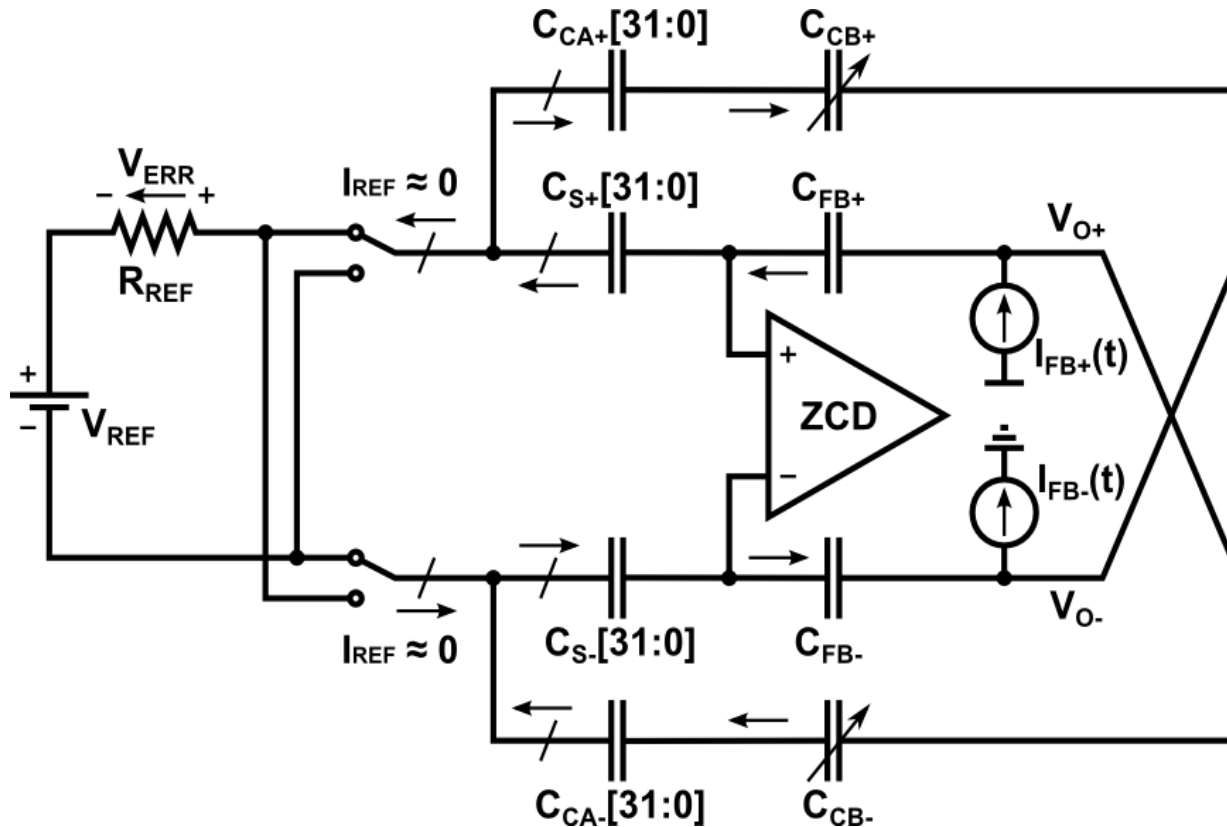
Reference Current Challenges (2)

ZCBC ADC



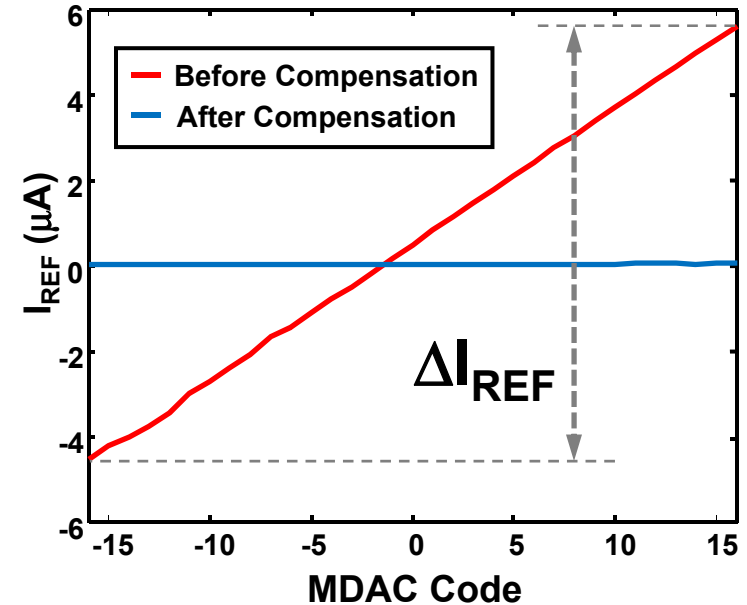
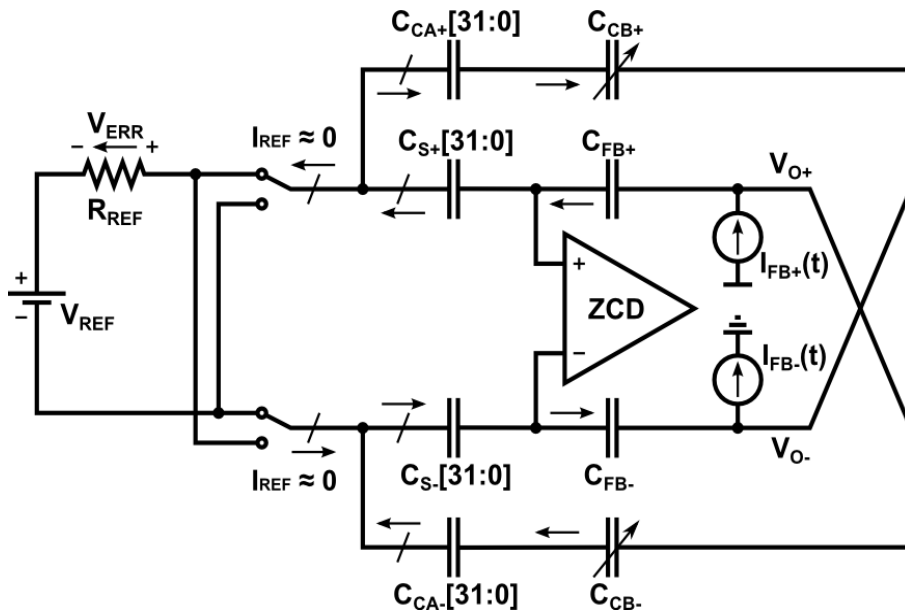
- I_{REF} is a function of output ramp and MDAC data
- At zero-crossing, I_{REF} is only a function of MDAC data
- V_{ERR} causes data-dependent modulation of effective $V_{REF} \rightarrow$ Second-order bowing

Reference Current Compensation (1)



- **Replica cross-coupled capacitors cancel I_{REF} into V_{REF} buffer**
- **Small area penalty for C_{CA} and C_{CB}**

Reference Current Compensation (2)



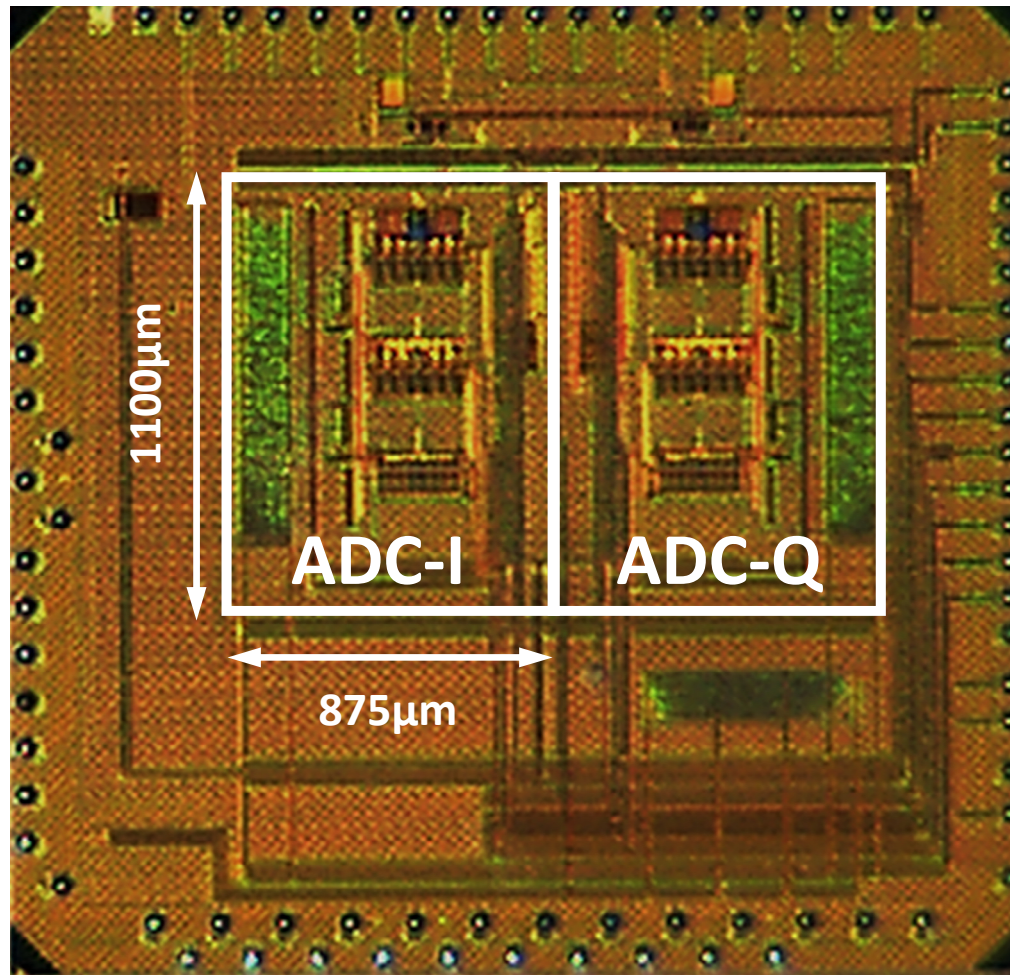
- On-chip V_{REF} buffer has significant output impedance
- ΔI_{REF} causes $>3\text{LSB}$ error (before comp.)
 $<0.02\text{LSB}$ error (after comp.)

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Die Photograph

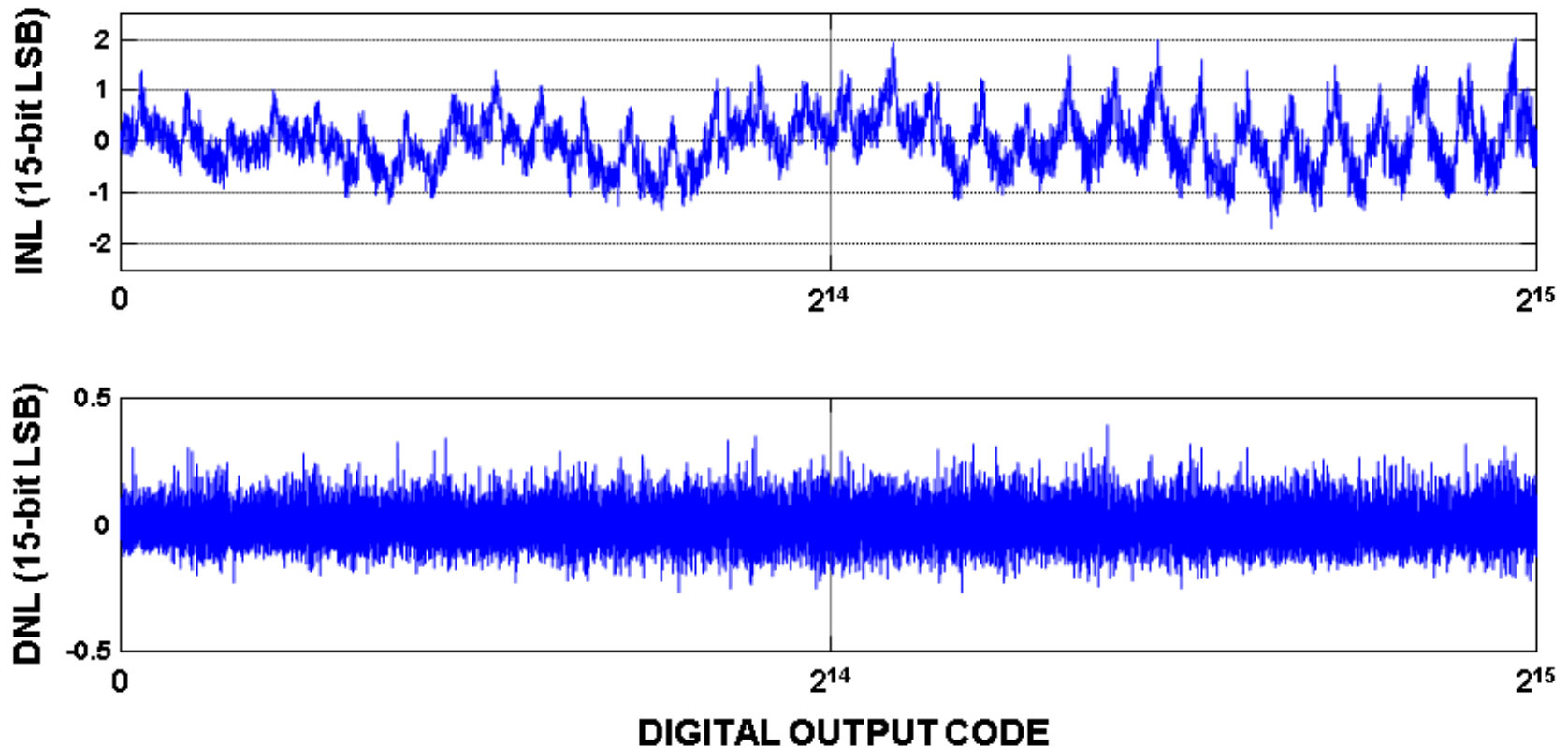
- Process: 130nm single-poly 6-metal CMOS



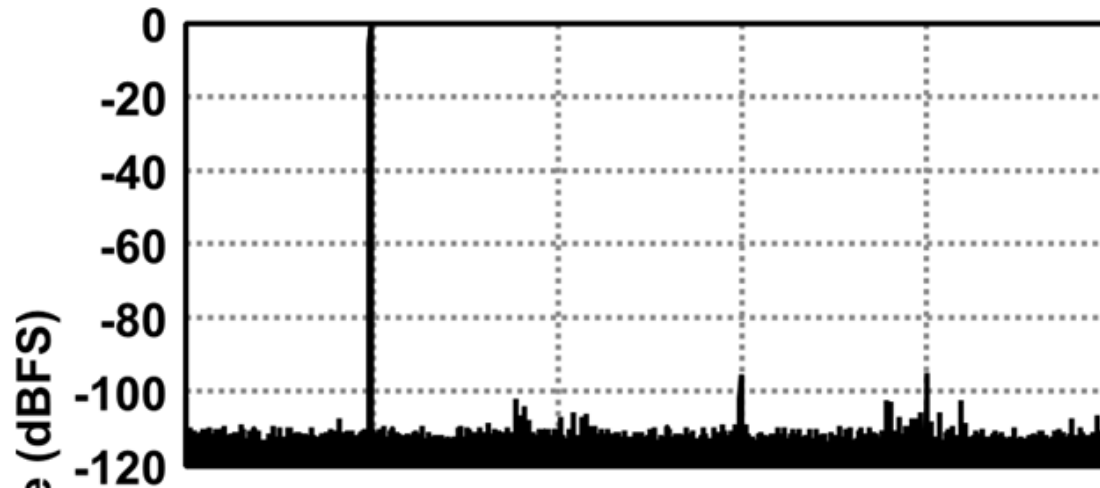
11.6: A 21mW 15b 48MS/s Zero-Crossing Pipeline ADC in 0.13μm CMOS with 74dB SNDR

Measurement: INL and DNL

- $F_{IN} = 5\text{MHz}$ and $F_S = 48\text{MHz}$



Measurement: Output Spectrum

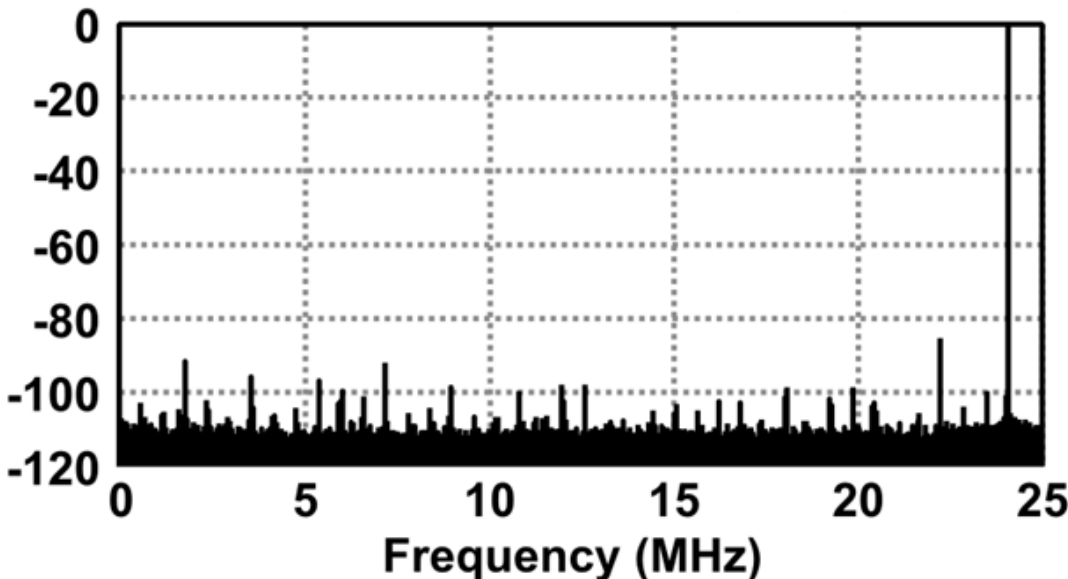


$F_S = 50\text{MHz}$

$F_{IN} = 5\text{MHz}$

SFDR = 93.5dBc

SNDR = 74.5dBFS



$F_S = 50\text{MHz}$

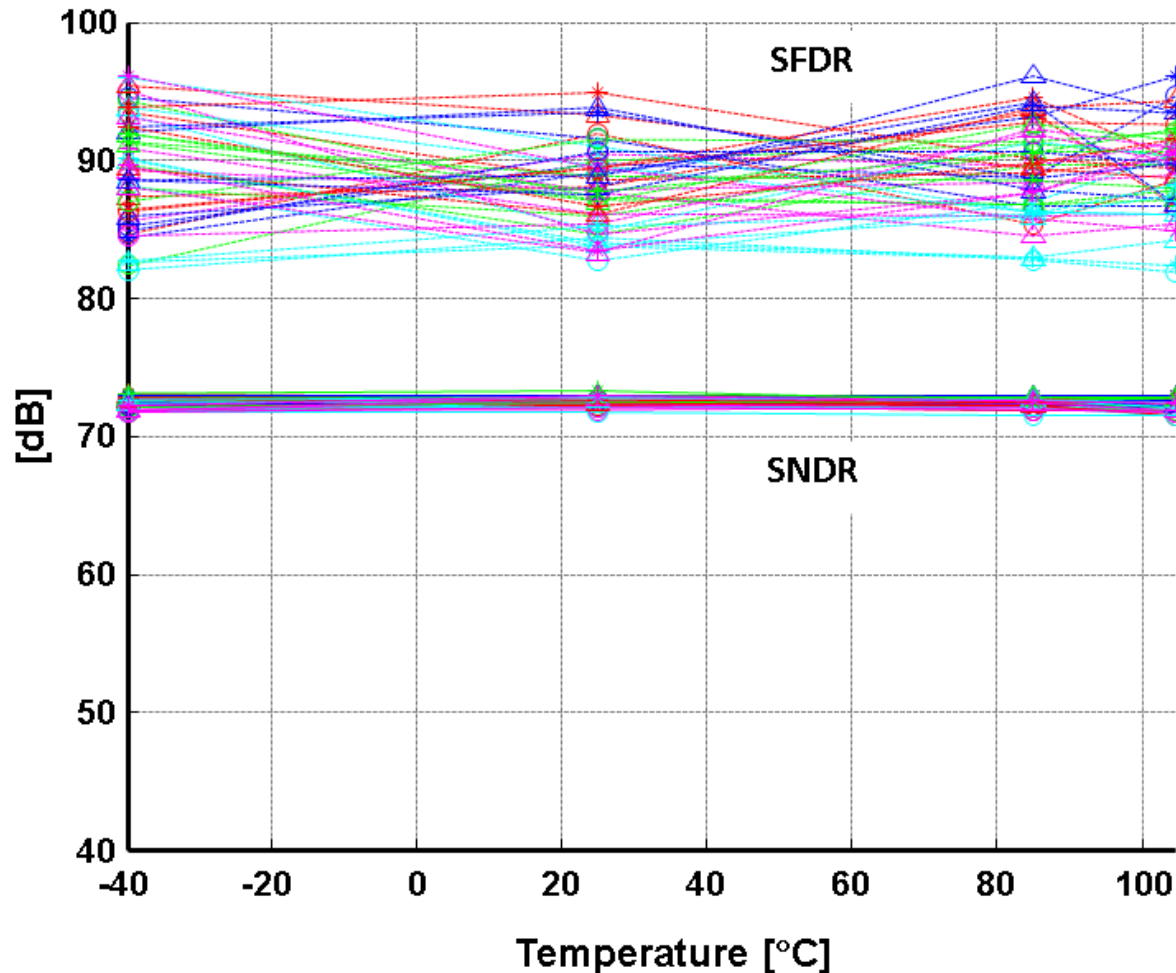
$F_{IN} = 24.1\text{MHz}$

SFDR = 84.2dBc

SNDR = 73.1dBFS

Measurement: PVT Performance

- 15 parts measured: 5 TT, 5 SS, 5 FF
- $F_{IN} = 10\text{MHz}$ and $F_S = 48\text{MHz}$, supply Δ : $\pm 10\%$



Performance Summary

	This Work	ISSCC 2013 [2]	ISSCC 2011 [3]	ESSCIRC'11 [4]
Technology	130nm CMOS	65nm CMOS	180nm CMOS	65nm CMOS
Architecture	ZCBC Pipeline	Interleaved SAR	Opamp Pipeline	ZCBC Pipeline
Resolution	15b	14b	16b	12b
Conversion Rate	50MS/s	80MS/s	80MS/s	50MS/s
Input Signal Range	2V _{p-p,diff}	2.4V _{p-p,diff}	-	1.67V _{p-p,diff}
SNDR	74.5dBFS @ 5MHz 73.1dBFS @ 24MHz	73.6dB @ 5MHz 71.3dB @ 40MHz	77.6dB @ 9.7MHz	67.7dB @ 23.9MHz
SFDR	95dBc @ 5MHz 84.2dBc @ 24.1MHz	85.7dB @ 5MHz ≥80.3dB @ 40MHz	95dB @ 9.7MHz	85.8dB @ 23.9MHz
Power Consumption	21.6mW	31.1mW	100mW	4.1mW
FOM1 [= SNDR + 10log ₁₀ (f _s /2/P)]	165.1dB	164.7dB	163.6dB	165.6dB
FOM2 [= P/(2 ^{ENOB} × f _s /2)]	99fJ/step	99fJ/step	201fJ/step	41fJ/step

[2] R Kapusta, "A 14b 80MS/s SAR ADC with 73.6dB SNDR in 65nm CMOS," ISSCC 2013

[3] J. Brunsilius, "A 16b 80MS/s 100mW 77.6dB SNR CMOS pipeline ADC," ISSCC 2011

[4] S. Lee, "A 12b 5-to-50MS/s 0.5V-to-1V voltage scalable zero crossing based pipelined ADC," ESSCIRC 2011

11.6: A 21mW 15b 48MS/s Zero-Crossing Pipeline ADC in 0.13μm CMOS with 74dB SNDR

Conclusion

- **A ZCBC pipeline ADC with SNDR of 74dB was realized in 130nm CMOS**
- **Robust performance over PVT can be achieved by using the following design techniques:**
 - **High-resolution stage with two-step conversion**
 - **Coarse phase threshold control in background**
 - **Reference current compensation during charge transfer**
- **The FOM of the ADC including digital and reference buffer was >165dB at 48MS/s with 5MHz input**

A 240mW 16b 3.2GS/s DAC in 65nm CMOS with $<-80\text{dBc}$ IM3 up to 600MHz

Hans Van de Vel, Joost Briaire, Corné Bastiaansen,
Pieter van Beek, Govert Geelen, Harrie Gunnink,
Yongjie Jin, Mustafa Kaba, Kerong Luo, Edward
Paulus, Bang Pham, William Relyveld, Peter Zijlstra

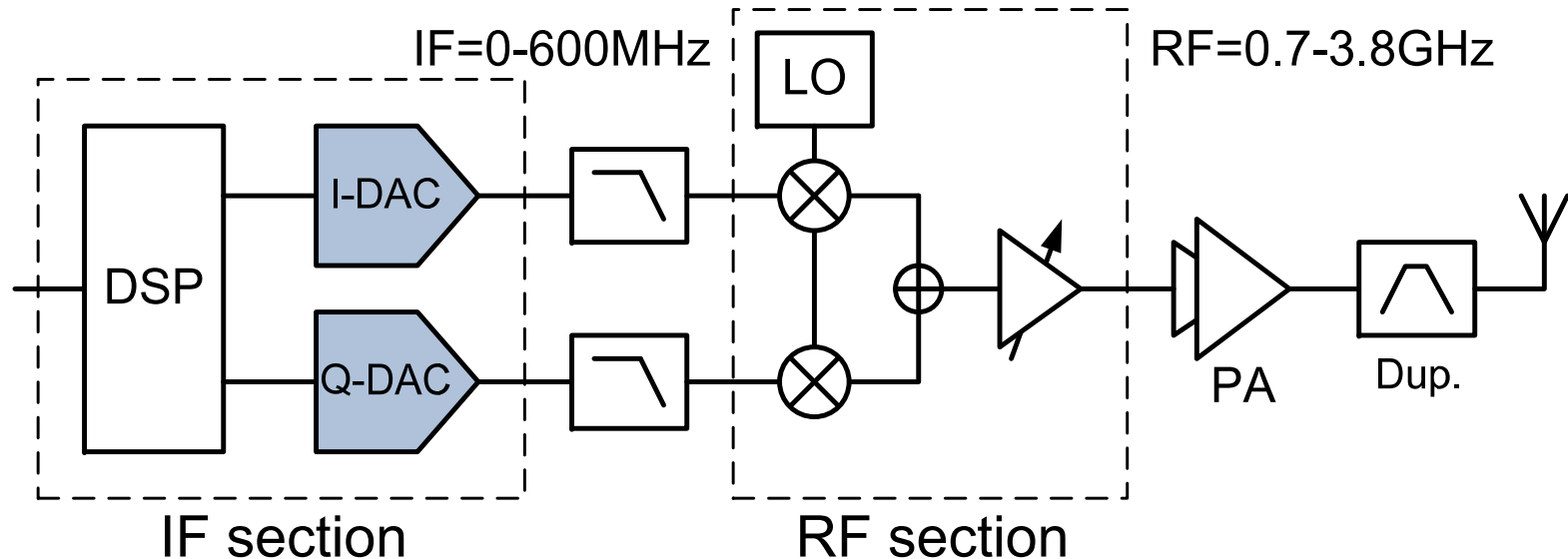


Integrated Device Technology
Eindhoven, The Netherlands

Outline

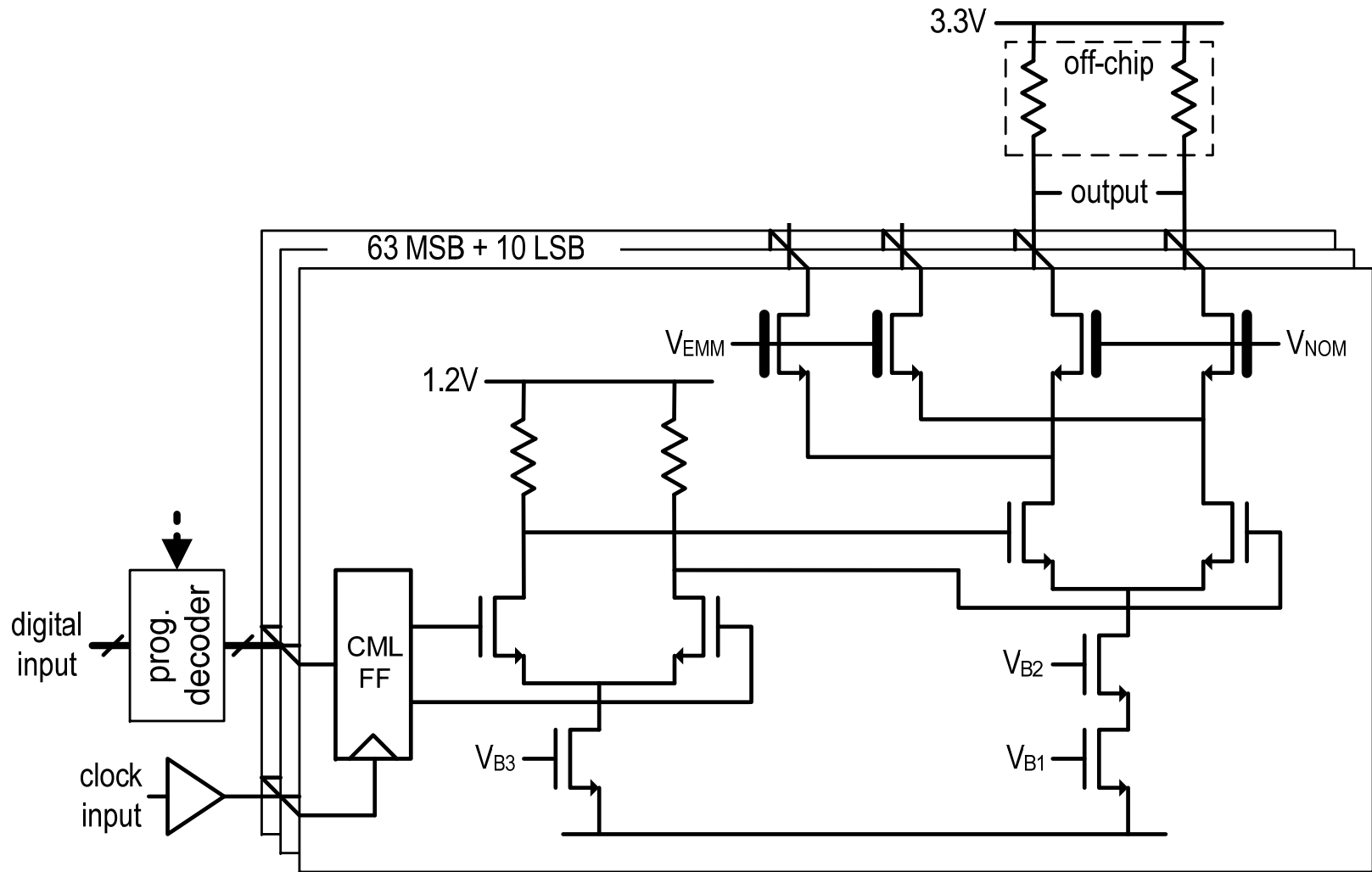
- Wireless infrastructure
- DAC architecture
- Mismatch calibration
- Circuit implementation
- Measurement results
- Conclusions

Wireless infrastructure systems

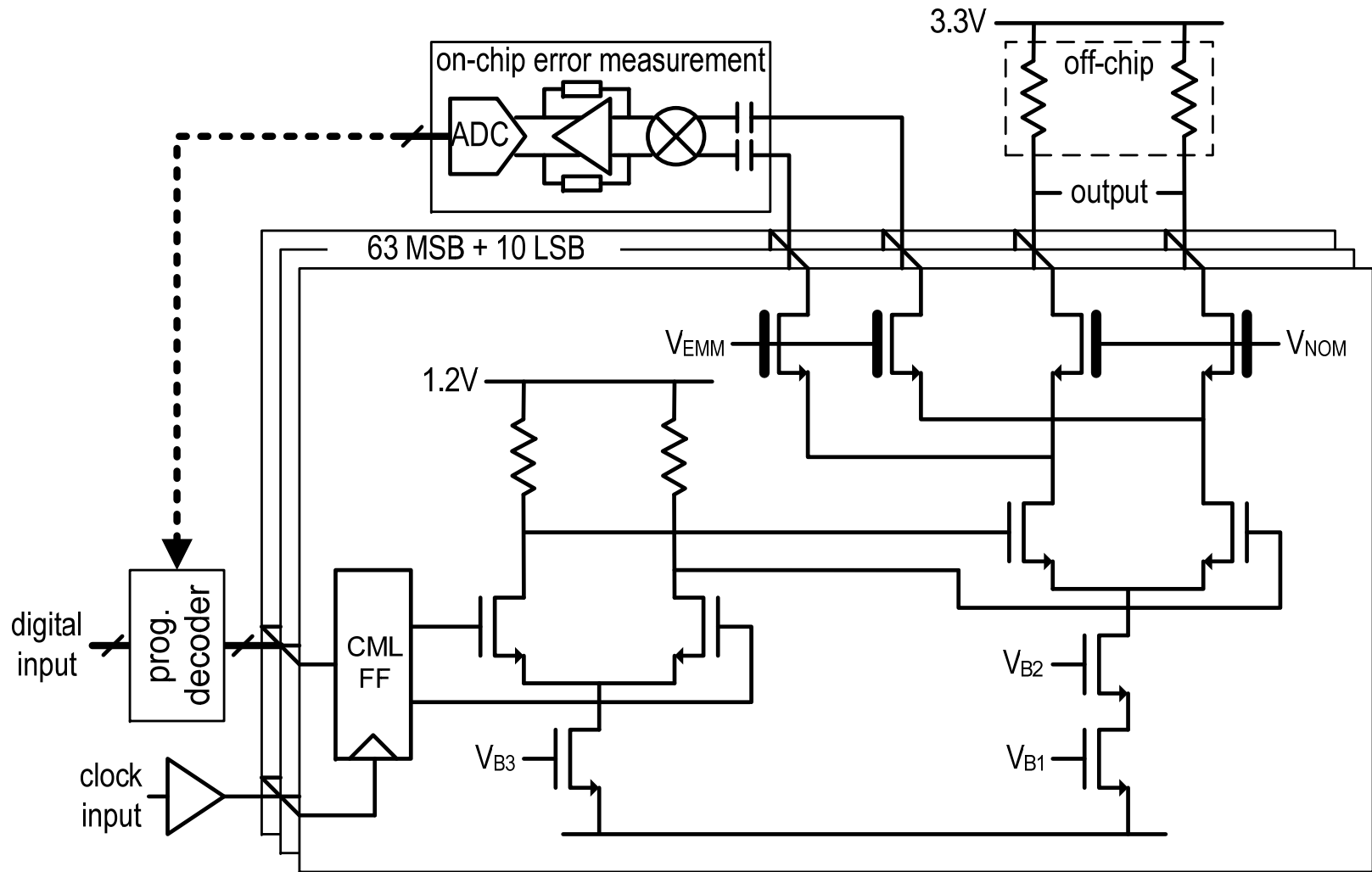


- Super-heterodyne transmitter with DACs at up to 600MHz IF
- LTE demands high spectral purity: $IM3 < -80dBc$
- Integration of complete IF section demands low power dissipation of DACs and DSP

Current-steering DAC architecture



Current-steering DAC architecture



Unit matching errors


DAC linearity impaired by 3 dimensions of matching errors

- Low f_{sig} : Amplitude
- High f_{sig} : Timing = delay and duty-cycle

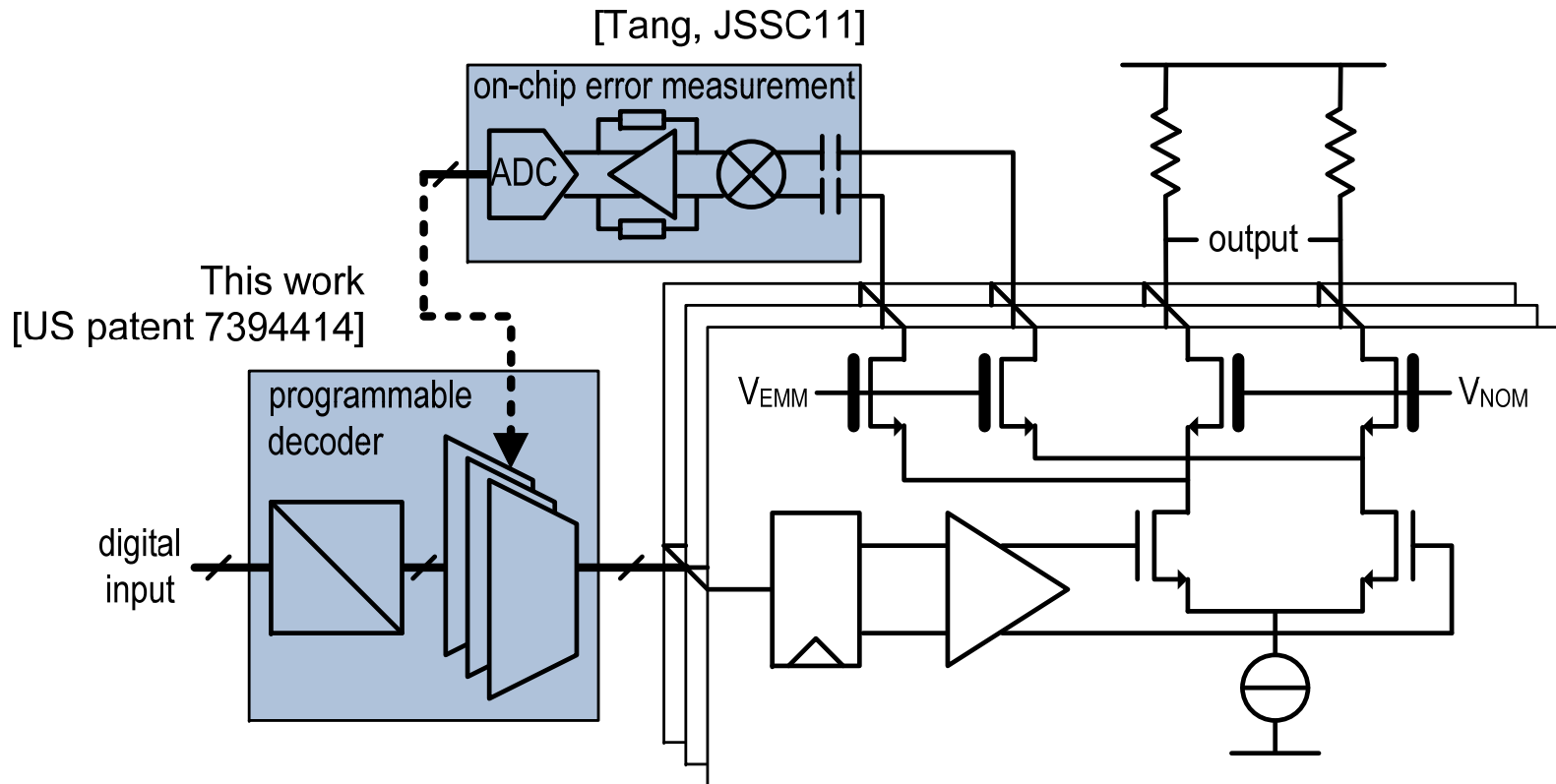
Minimize by design:

- Large current sources
- Fast switches \Rightarrow high power dissipation 

Minimize through calibration:

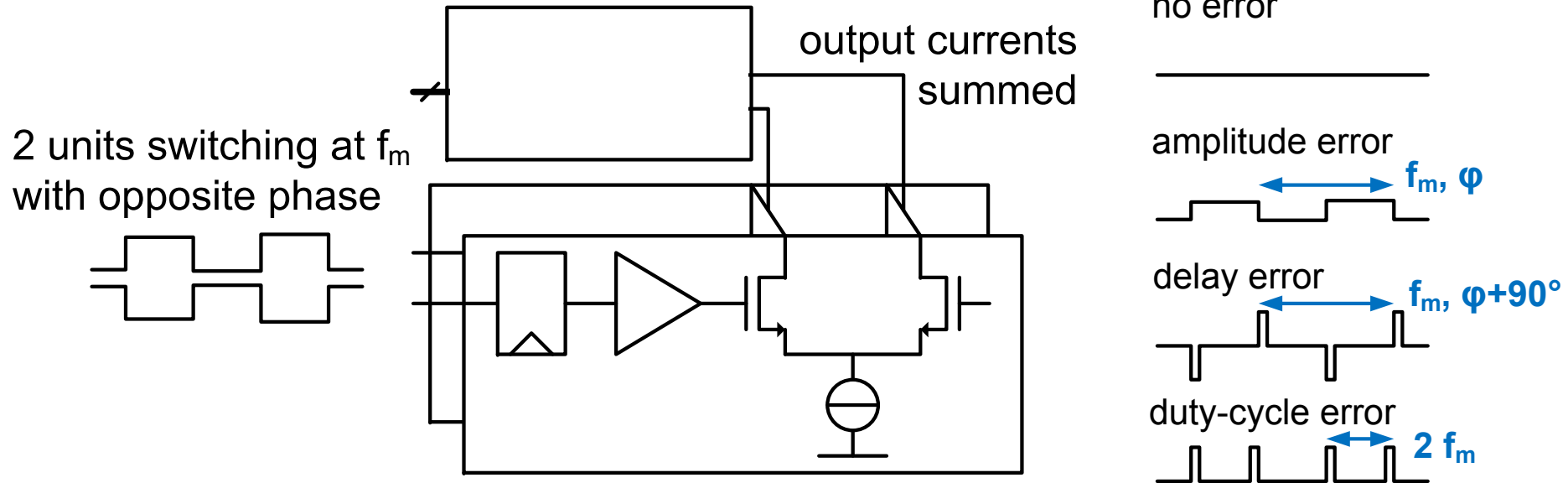
- Small current sources
- Low power dissipation in switch drivers 

Mismatch calibration

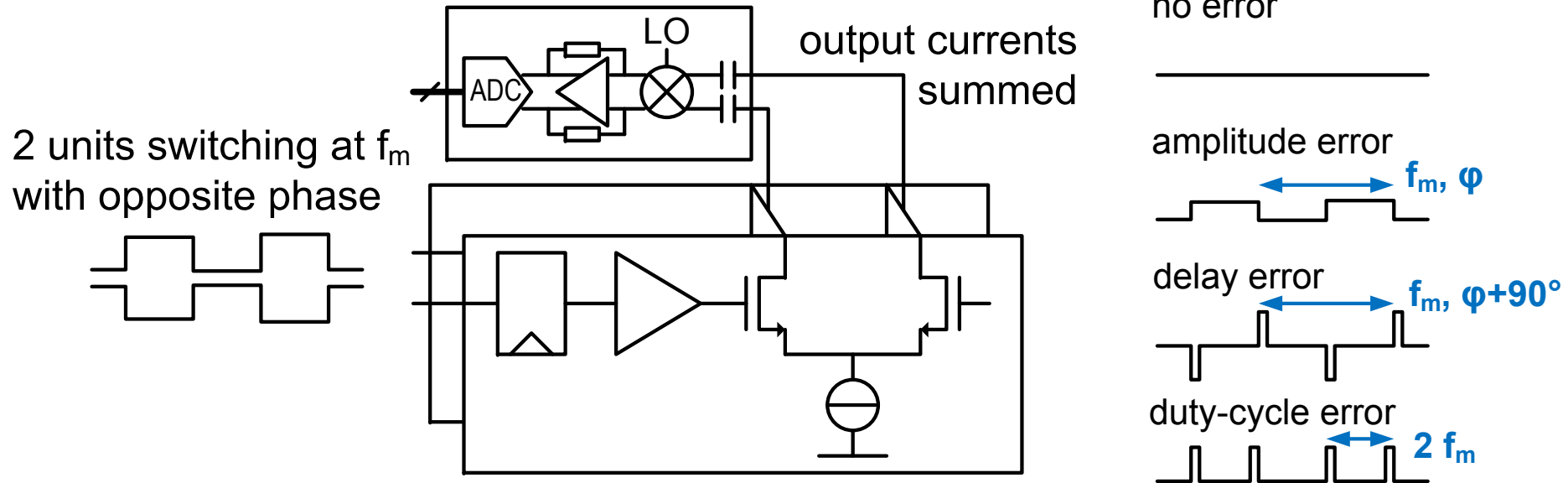


- Errors measured on-chip and digitized
- Errors corrected through programming digital MUXes – no analog tuning

On-chip error measurement



On-chip error measurement



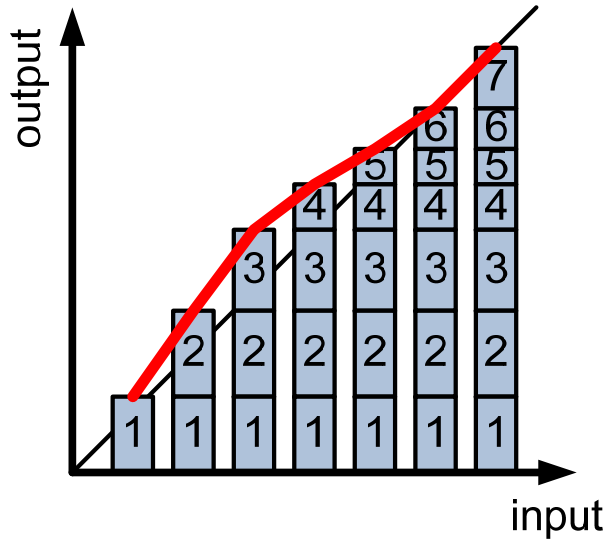
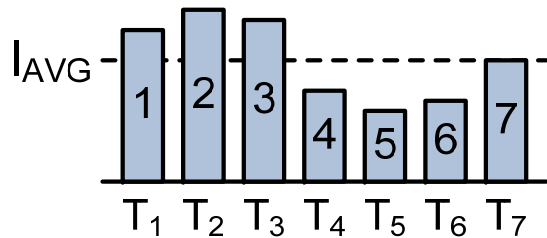
Error signal down-converted to DC, filtered and digitized

- $f_{LO} = f_m$ & $\varphi_{LO} = \varphi \Rightarrow$ amplitude error
- $f_{LO} = f_m$ & $\varphi_{LO} = \varphi + 90^\circ \Rightarrow$ delay error
- $f_{LO} = 2 f_m \Rightarrow$ duty-cycle error

[Tang, JSSC11]

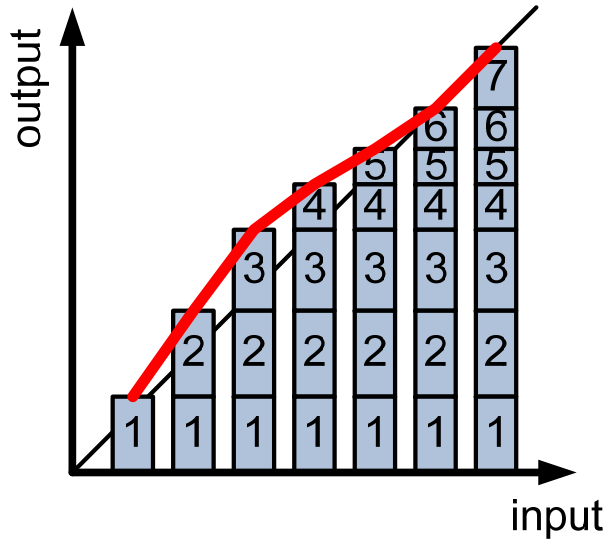
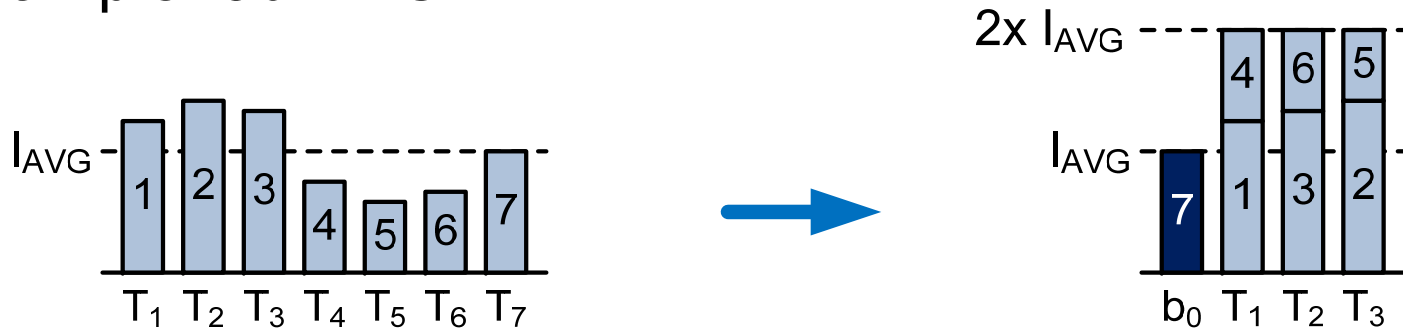
Sort-and-combine calibration

Example: 3b DAC



Sort-and-combine calibration

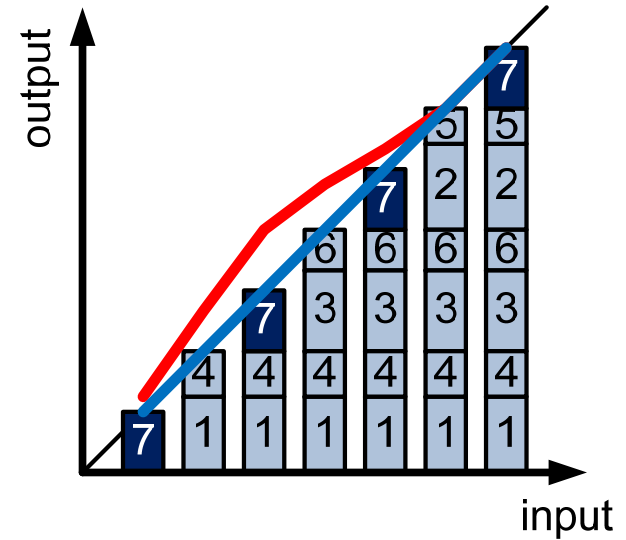
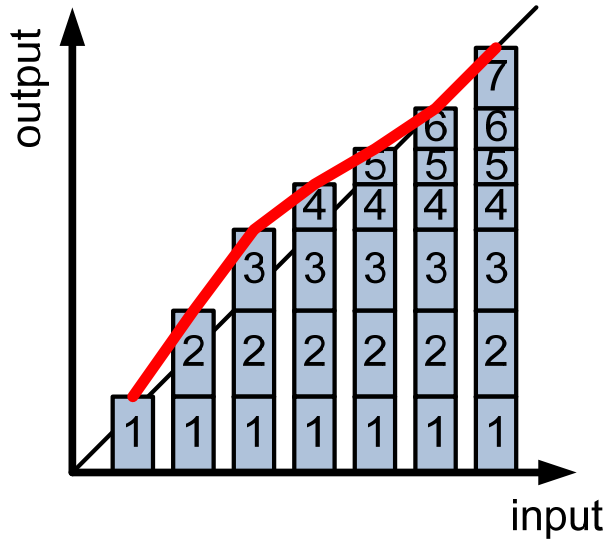
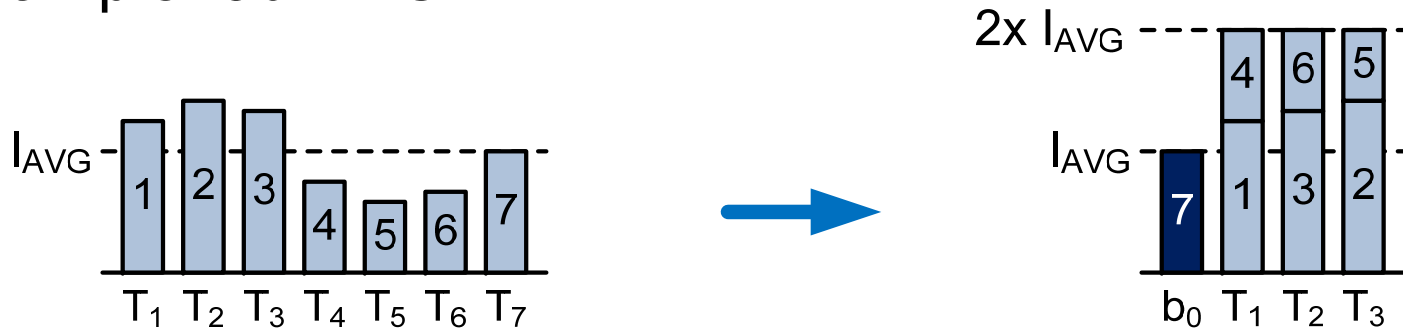
Example: 3b DAC



[US patent 7394414]

Sort-and-combine calibration

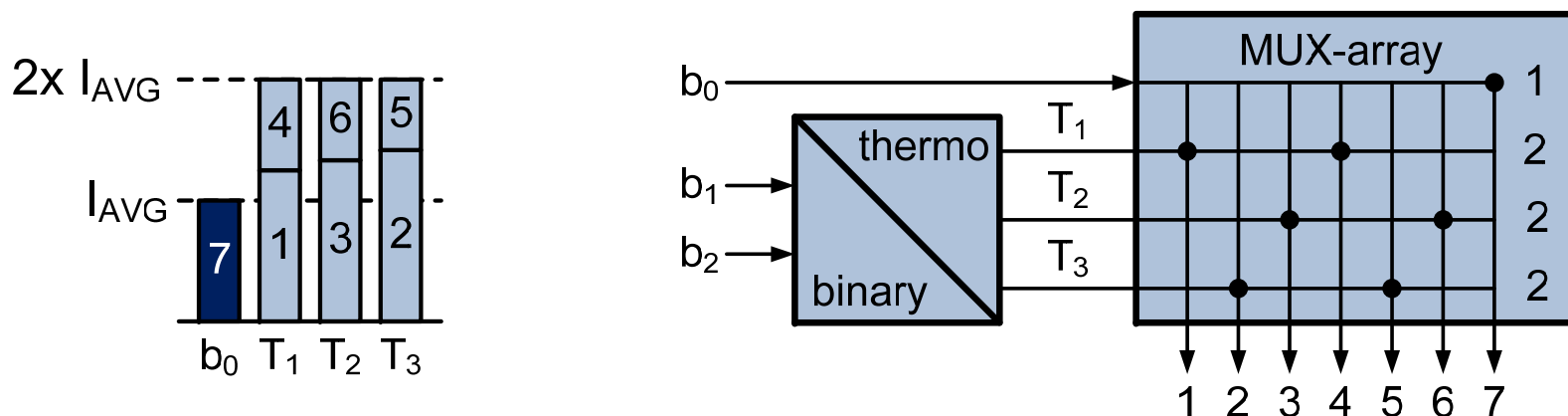
Example: 3b DAC



[US patent 7394414]

Programmable decoder

Sort-and-combine to combinations of 2 units:



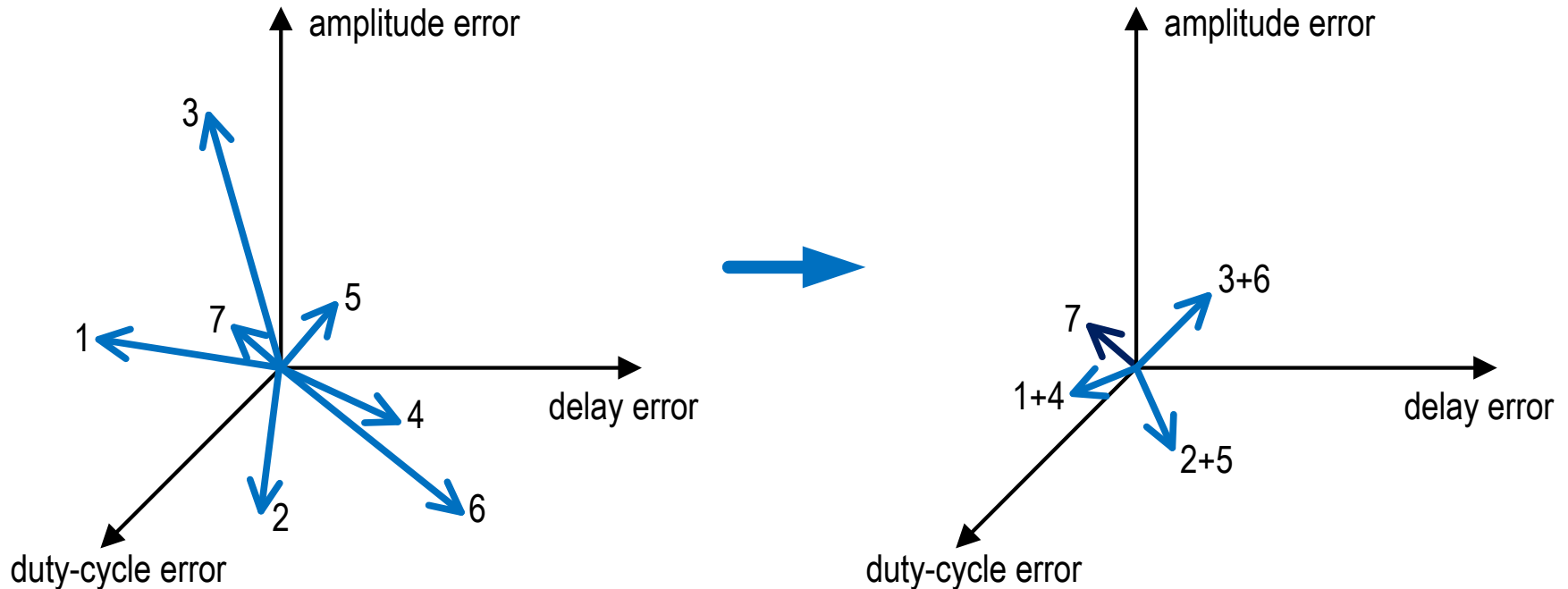
Repeat sort-and-combine to combinations of 4 units

⇒ Further error reduction

⇒ Programmable decoder reconfigured:
MSB passed by 4 MUXes

3D sort-and-combine

3D unit matching errors represented as 3D error vectors:



3D sort-and-combine (3D-SC) calibration:

- Select unit with smallest error vector (unit 7)
- Sort-and-combine other units to reduce error sum vectors

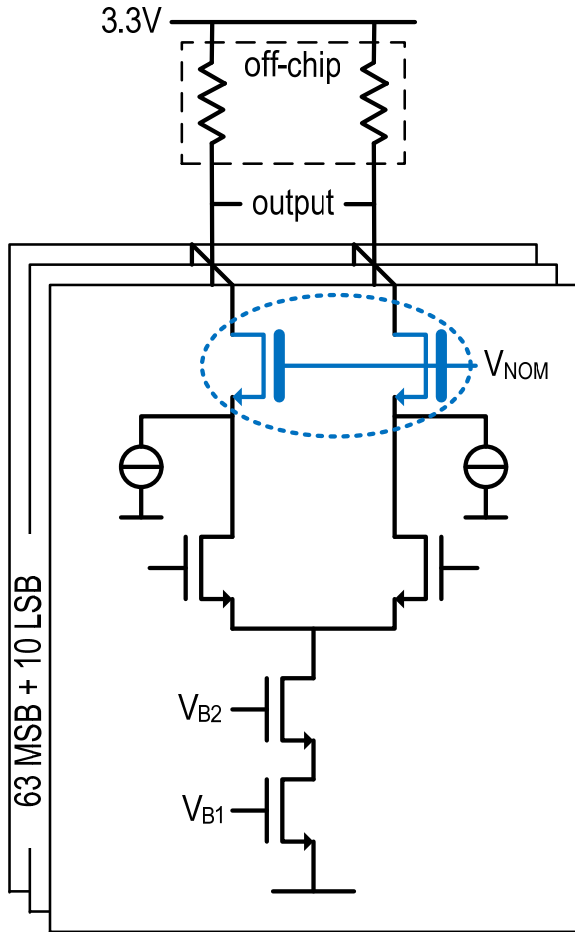
3D-SC calibrated DAC

- Change in segmentation for 63 MSB units / 10 LSB units
 - Before 3D-SC: 6b thermometer / 10b binary
 - After 3D-SC: 4b thermometer / 12b binary (combinations of 4 units)
- Errors are reduced and not randomized (cf. DEM)
⇒ no noise penalty
- Only digital MUX-array adds to power dissipation
⇒ limited power penalty

CML latches and switch drivers

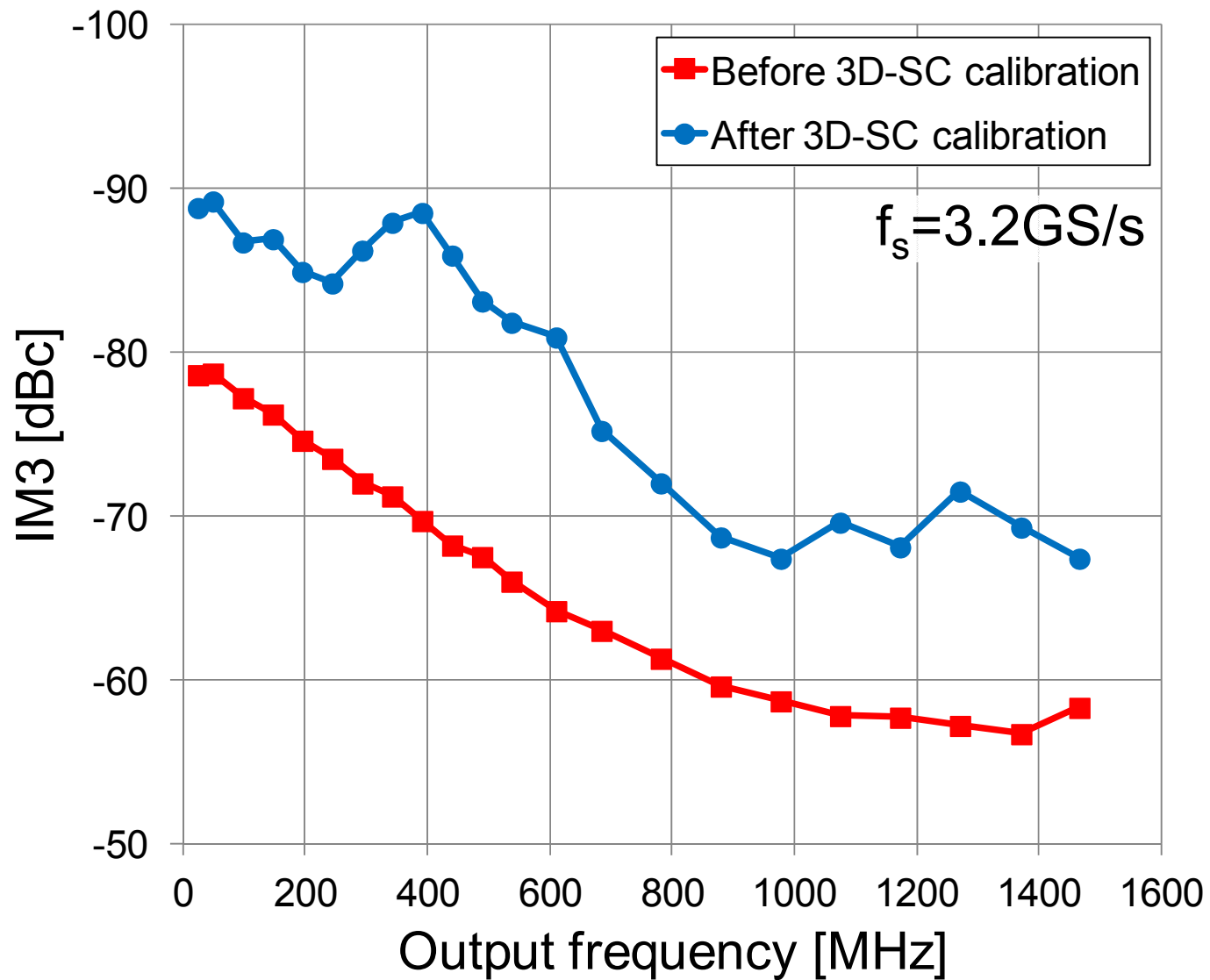
- Static biasing
 - ⇒ low supply bounce
- Low swing
 - ⇒ low switch gate-drain feed-through
 - ⇒ low switch channel injection
- High crossing point
 - ⇒ minimal glitch at switch common source node

Thick-oxide switch cascodes

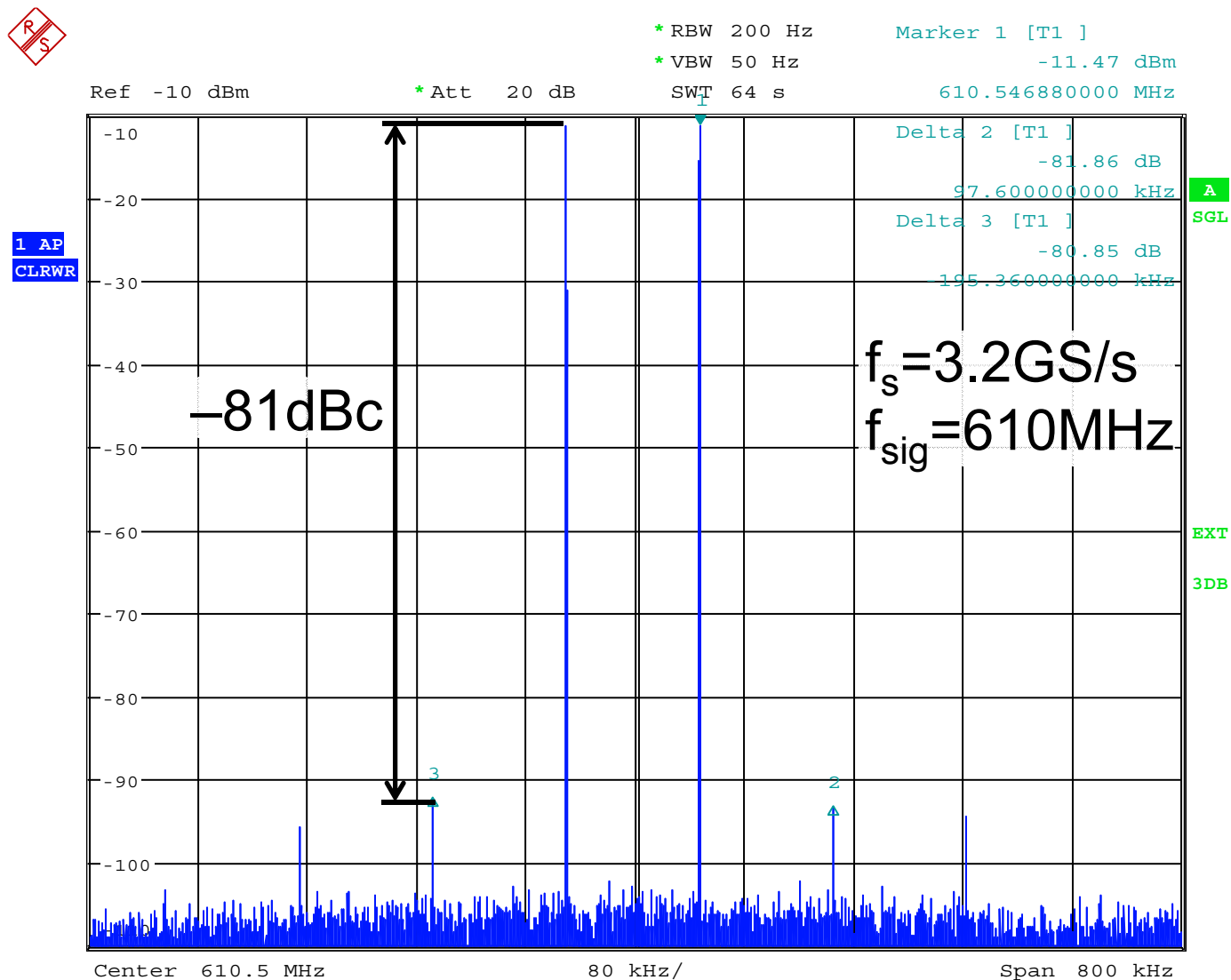


- Reduce feed-through of output signal to switch common source node
- Protect thin-oxide switches from 3.3V supply
- Reduce output impedance modulation

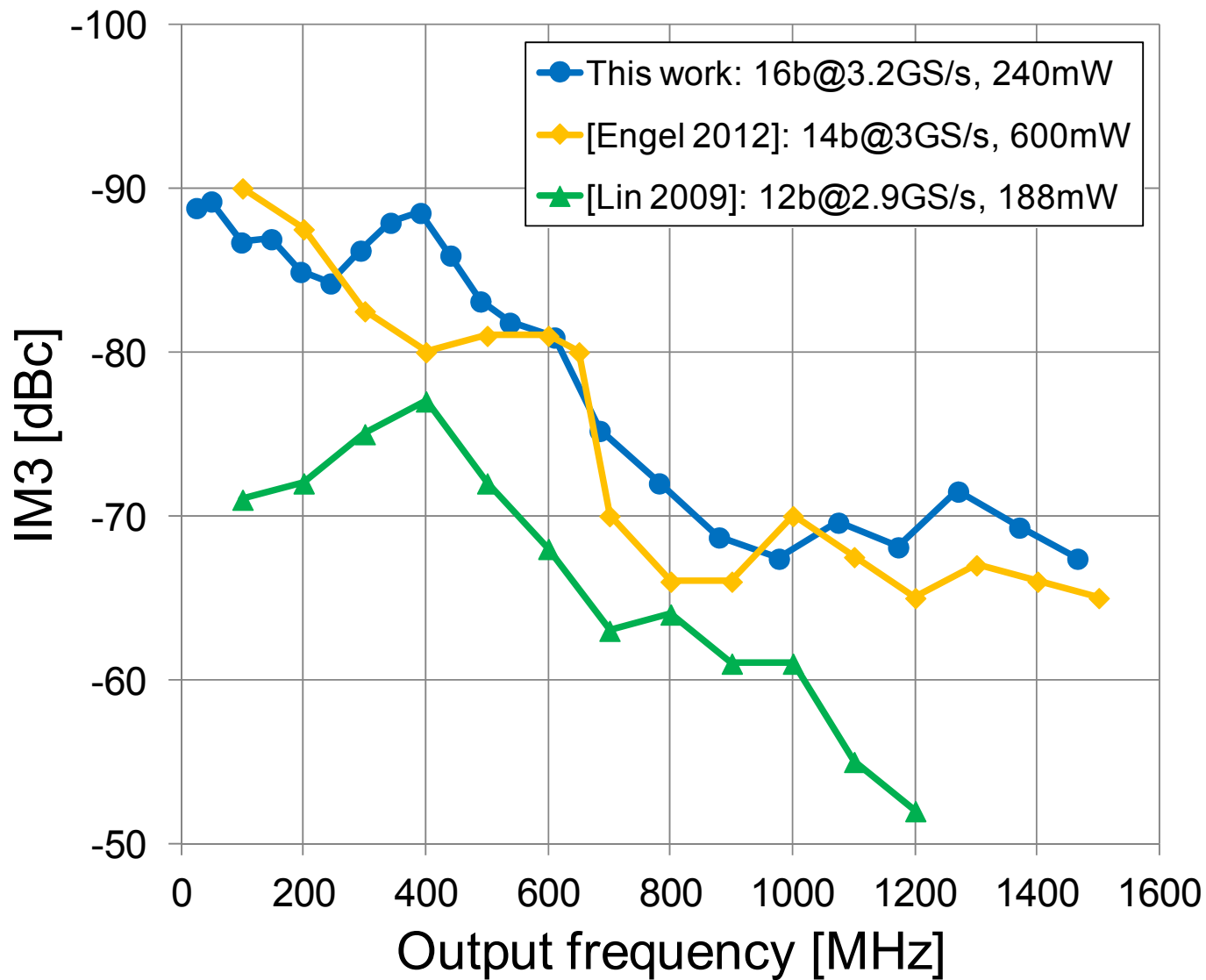
Measured IM3



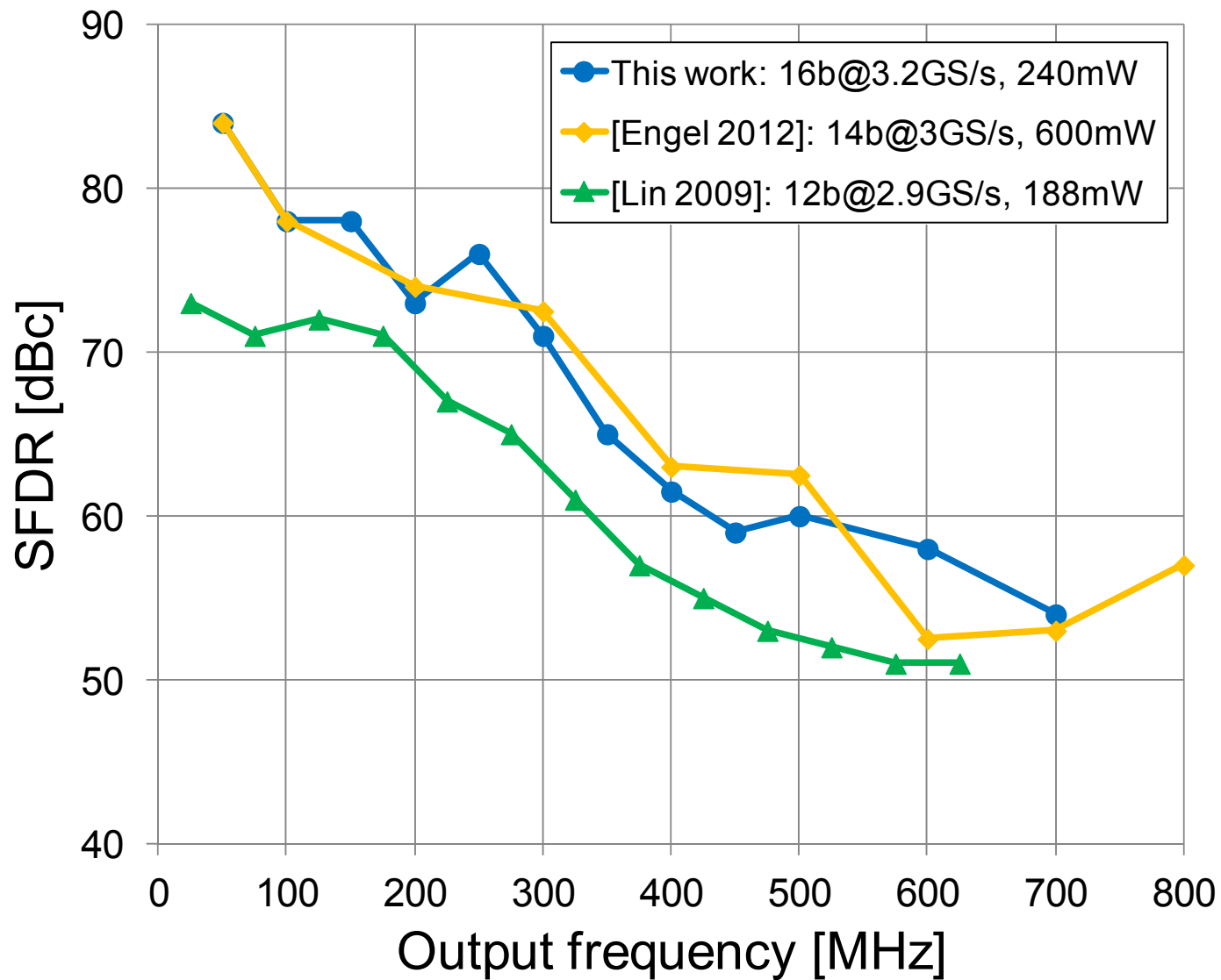
Measured spectrum



Performance comparison



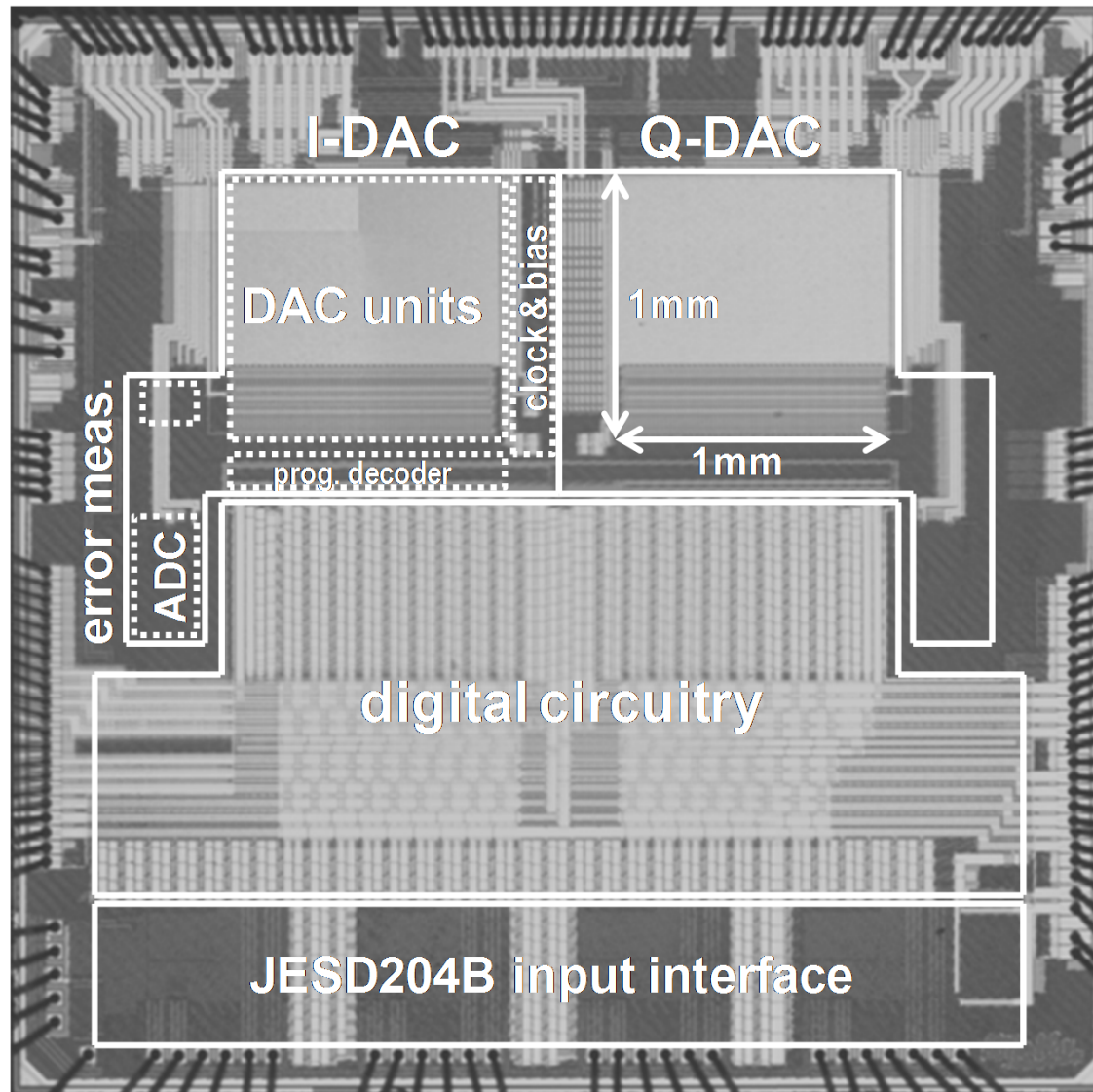
Measured SFDR



Performance summary

	This work	[Engel 2012]	[Lin 2009]
Technology	65nm CMOS	0.18 μ m CMOS	65nm CMOS
Supply (V)	1.2 / 3.3	1.8 / 3.3	1 / 2.5
Resolution	16	14	12
Sampling rate (GS/s)	3.2	3	2.9
Power (mW)	240	600	188
I_{load} (mA)	20 (max. 40)	20	50
$V_{pp-diff}$ (V)	1 (max. 2)	1	2.5
$BW_{IM3 < -80dBc}$ (MHz)	610	650	/
IM3 at 600MHz (dBc)	-81	-81	-68
SFDR at 600MHz (dBc)	58	53	51
NSD (dBm/Hz)	-168	/	/

Die micrograph



Conclusions

- Amplitude and timing mismatch can be calibrated through 3-dimensional sorting-and-combining
Improves linearity up to high frequencies &
Enables low power dissipation
- Calibrated DAC achieves -80dBc IM3 up to 600MHz with 240mW power dissipation
- Low-power 65nm CMOS DAC enables single-chip IF transmit section for wireless infrastructure